SHARP SERVICE MANUAL

CODE : 00ZSL5500SM/E

Personal Mobile Tool

MODEL SL-5500

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PARTS GUIDE

Parts marked with "⚠" are important for maintaining the safety of the set. be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

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CHAPTER 1. SPECIFICATIONS

SL-5500, a Sharp Linux/Java based multimedia PDA, implements Linux 2.4.x (Embedix by Lineo Inc.) as its operating system, Qt/Embedded and Qt Palmtop Environment (both by Trolltech) for its Linux application platform, and further implements PersonalJava environment (Jeode by Insignia Solutions) to execute PersonalJava applications.

By implementing both Linux and Java, which are open and standard platform, anyone may develop application software for the SL-5500 by using existing and easily available tools.

1. PRODUCT SPECIFICATIONS

1-1. BASIC SPECIFICATIONS

The following table provides a brief overview of SL-5500 hardware specifications.

CPU	StrongARM (SA-1110, 206 MHz)
Platform	Linux 2.4 (Embedix) / PersonalJava (Jeode)
Display	Reflective TFT LCD with Front light (Touch-sensitive panel supported) 3.5" with 240 x 320 pixels, 65,536 colors
Memory	ROM: 16MB FLASH for OS, Applications, Driver, etc. RAM: 64MB SDRAM
Input Device	Touch panel, Type-writer keyboard
Character Input	QWERTY Keyboard with a slide cover, Software keyboard, hand-writing, Pick board (similar to cellular phone input)

1-2. FUNCTIONAL SPECIFICATIONS

The following table provides a brief overview of SL-5500 functional specifications.

Internet Mail	POP3 / IMAP4 / SMTP File attachment capability
WWW Browser	Opera (HTML4.0, JavaScript1.3, CSS1, cookie)
Media Player (Multimedia Files)	MPEG1 (Movie: MPEG1 compliant) MP3 (Audio: MP3 compliant)
Palmtop (Launcher)	Tab bar: on the top of the screen containing Applications, Games, Jeode (PersonalJava runtime environment), Settings, and Documents. Launch bar: on the bottom with invoked application icons, migrated with Console, that provides Time, Battery monitor, and volume control.
Applications	Todo List, Calendar, Address Book, Text Editor, Image Viewer, Calculator, City Time, Clock, Help Browser, Media Player, Opera Browser, E-Mail, System info, Voice Recorder, Hancom Presenter, Hancom Sheet, Hancom Word
PC Synchronization	PC synchronization with Qtopia Desktop

1-3. COMMON SPECIFICATIONS

The following table provides a brief overview of SL-5500 common hardware specifications.

Power Supply	AC Adapter (bundled): 5.0V DC Replaceable Lithium-ion battery (bundled): 3.7V DC Memory backup battery (Built-in): 3.0V DC
Battery life	When the power of the SL-5500 is turned on at a temperature of under 25°C (75°F), with no peripheral device (including the CF memory card) connected, after the rechargeable battery (EA-BL06) is fully charged. • approx. 10 hours (when you display the Day view mode screen of the Calendar application continuously with the frontlight turned off.) • approx. 1 hour (when you play the mpeg 1 file continuously with the frontlight at its brightest level turned on.)
Data storage time	When the power of the SL-5500 is turned off at a temperature of under 25°C (75°F) after the brand-new battery is fully charged. • approx. 10 days When the operating battery is exhausted and the power can not be turned on. • approx. 1 day When the operating battery is not inserted after the rechargeable back-up battery is fully charged. • approx. 5 minutes
Number of charging and discharging of the operating battery life	Approx. 500 times. Note: The Battery life and storage time may vary depending on the usage.
Power Consumption	2.5 W (with battery) 6.2 W (with AC adapter)
Temperature Range	For operation: 0°C to 40°C (32°F to 104°F) For charging battery: 5°C to 35°C (37°F to 99°F)
Dimensions (when the slide cover is closed)	**Excluding the display protection cover** Approx. 74 (W) x 138 (D) x 18 (H) mm Approx. 2.9 (W) x 5.4 (D) x 0.7 (H) inches **Including the display protection cover (excluding protruding parts)** Approx. 74 (W) x 138 (D) x 21 (H) mm Approx. 2.9 (W) x 5.4 (D) x 0.8 (H) inches
Weight	Excluding display protection cover: Approx. 194 g (6.8 oz) Including display protection cover: Approx. 212 g (7.5 oz) Above values include battery, stylus, and CF Slot Protection Card
Bundled Accessories	Docking Station (USB direct coupled cable) AC adapter (P/N: EA-70, for IN 100-240 VAC) and Power Cord Lithium-Ion Battery (P/N: EA-BL06) Stylus, Display Protection Cover, CF Slot Protection Card

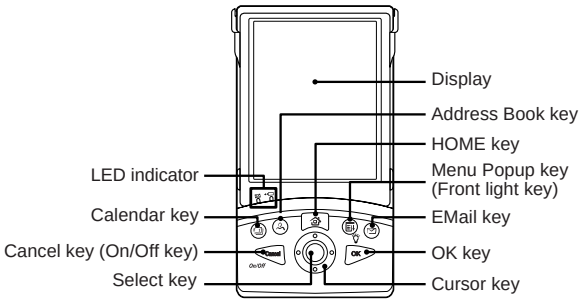
1-4. INTERFACE SPECIFICATIONS

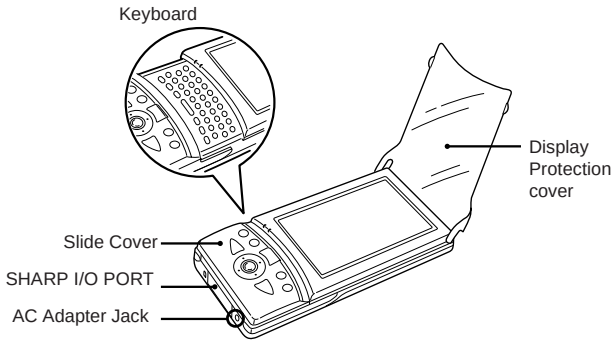
The following table provides a brief overview of SL-5500 hardware interface specifications.

Card Slot	CF type II x 1 (Compact Flash) SD card x 1 (no copyright protection feature)
I/O Port	Infrared (115.2 kbps, Link Distance 5 ~ 20cm) Serial port (Proprietary 16-pin) Serial/USB I/F (via docking station) port
Sound	Stereo Headphone Jack including Audio input (Mono) Buzzer

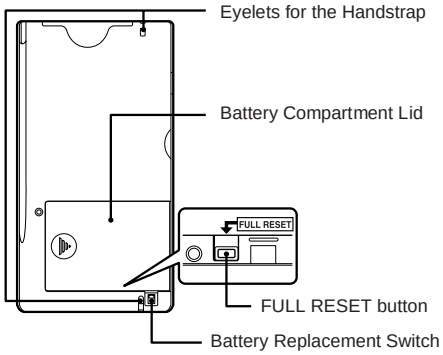
2. PART NAMES

Front

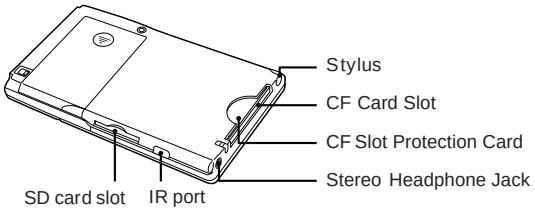




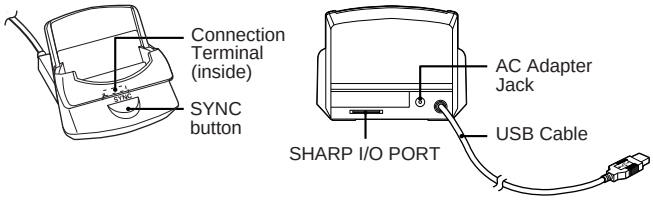
Back



Rear

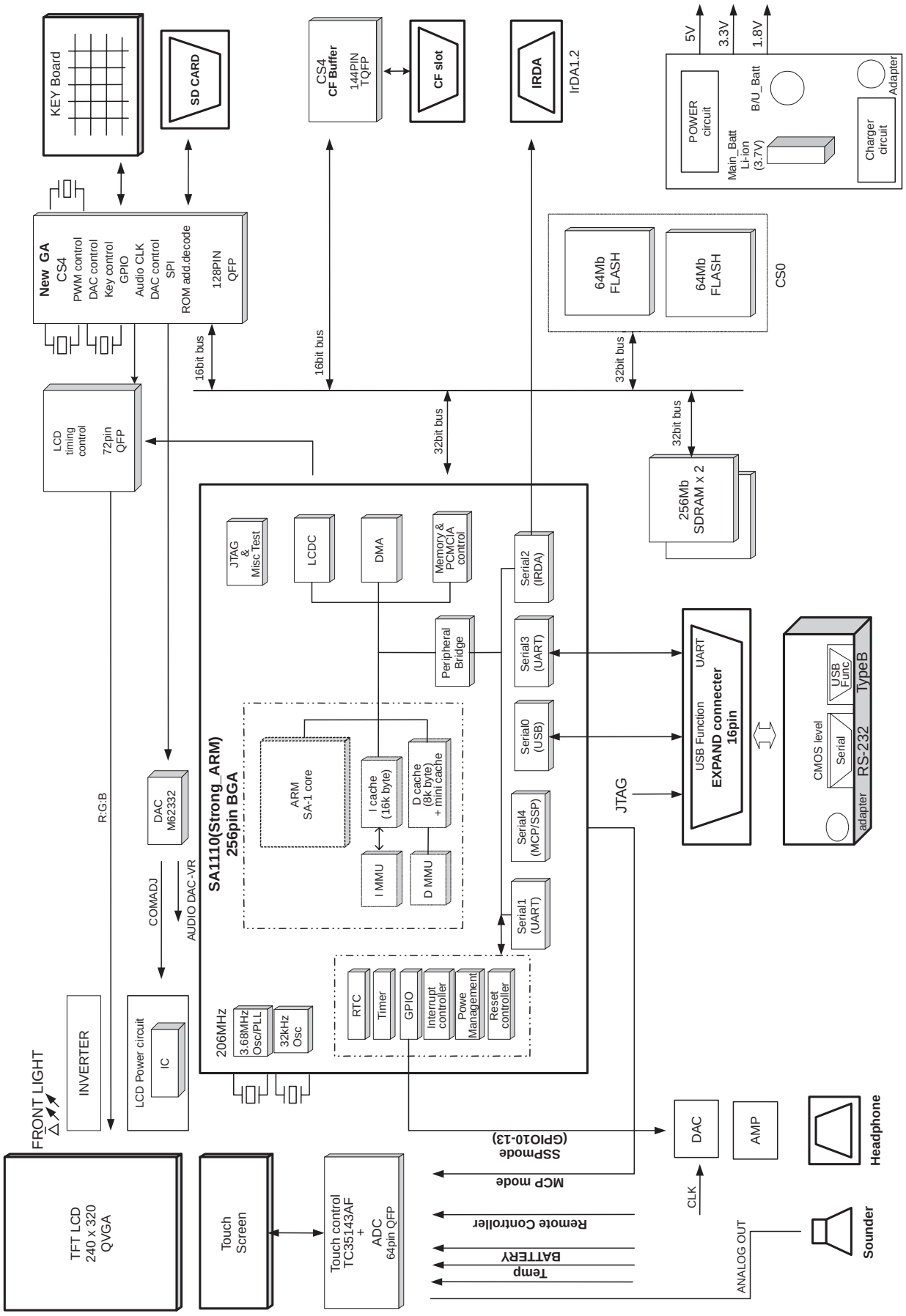


Dockng Station

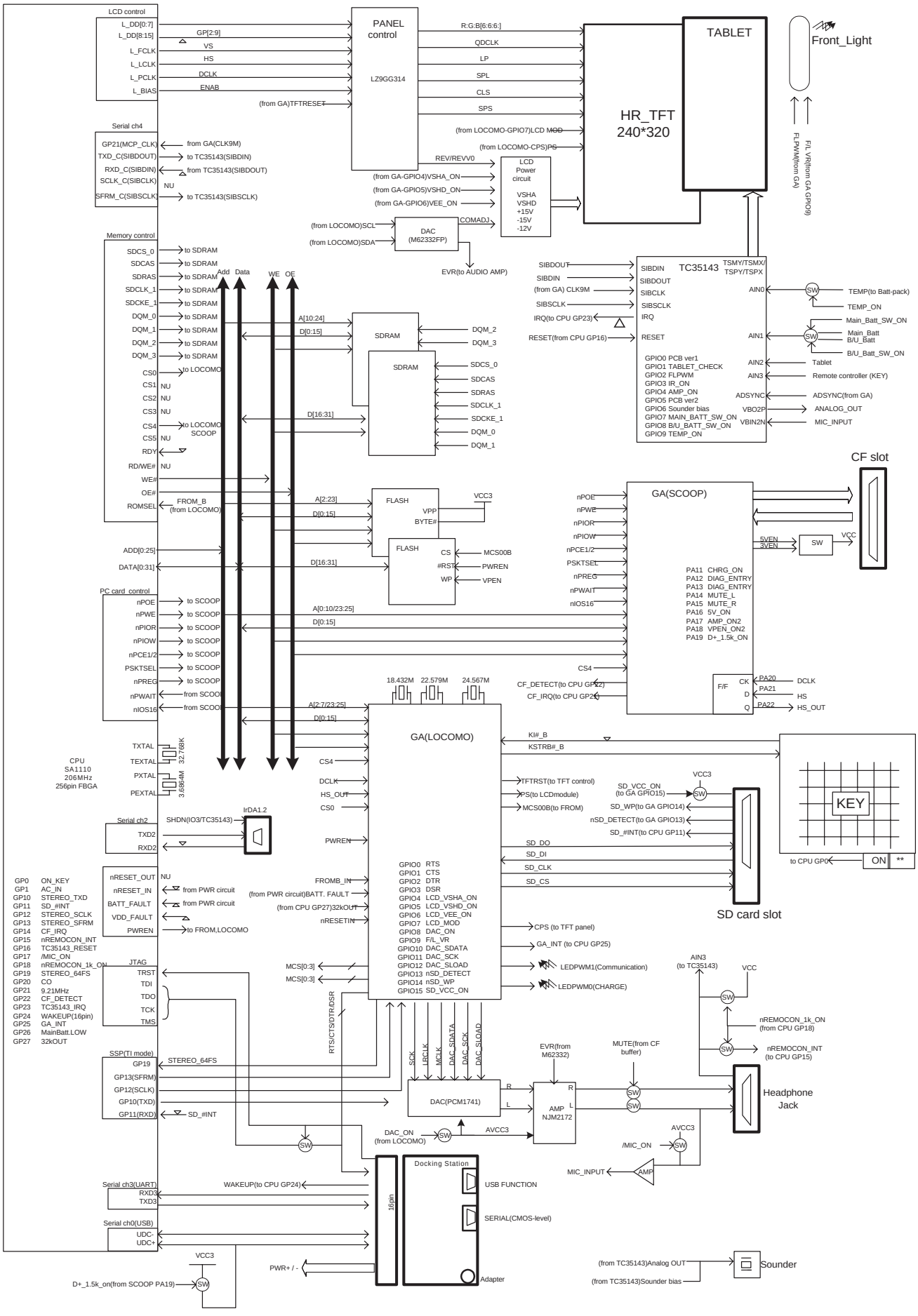


CHAPTER 2. HARDWARE DESCRIPTION

1-1. BLOCK DIAGRAM



1-2. DETAILED OF BLOCK DIAGRAM



2. DESCRIPTION OF LSI

2-1. CPU (SA-1110)

(1) GENERAL DESCRIPTION

The Intel StrongARM* SA-1110 Microprocessor (SA-1110) is a highly integrated communications microcontroller that incorporates a 32-bit StrongARM RISC processor core, system support logic, multiple comunication channels, an LCD controller, a memory and PCMCIA controller, and general-purpose I/O ports.

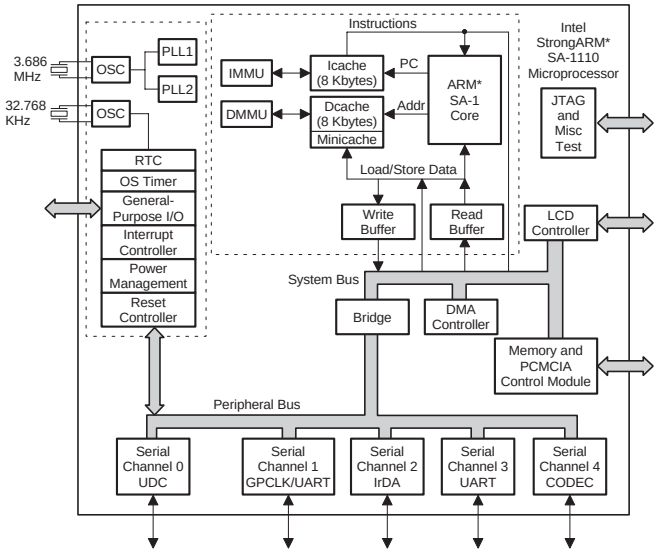
(2) FEATURES

- High Performance
  - – 150 Dhrystone 2.1 MIPS @ 133MHz
  - – 235 Dhrystone 2.1 MIPS @ 206MHz
- Low power (normal mode)*
  - – <240mW @ 1.55V/133MHz
  - – <400mW @ 1.75V/206MHz
- Integrated clock generation
  - – Internal phase-locked loop (PPL)
  - – 3.686MHz oscillator
  - – 32.768kHz oscillator
- Power-management features
  - – Normal (full-on) mode
  - – Idle (power-down) mode
  - – Sleep (power-down) mode
- Big and little endian operating modes
- 3.3V I/O interface
- 256-pin mini-BGA package (mBGA)
- 32-way set-associative caches
  - – 16Kbyte instruction cache
  - – 8Kbyte write-back data cache
- 32-entry memory-management units
  - – Maps 4Kbyte, 8Kbyte, or 1Mbyte
- Write buffer
  - – 8-entry, between 1 and 16bytes each
- Read buffer
  - – 4-entry, 1, 4, or 8 words
- Memory bus
  - – Interfaces to ROM, synchronous mask ROM (SMROM), Flash, SRAM, SRAM-like variable latency I/O, DRAM, and synchronous DRAM (SDRAM)
  - – Supports two PCMCIA sockets

* Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design.

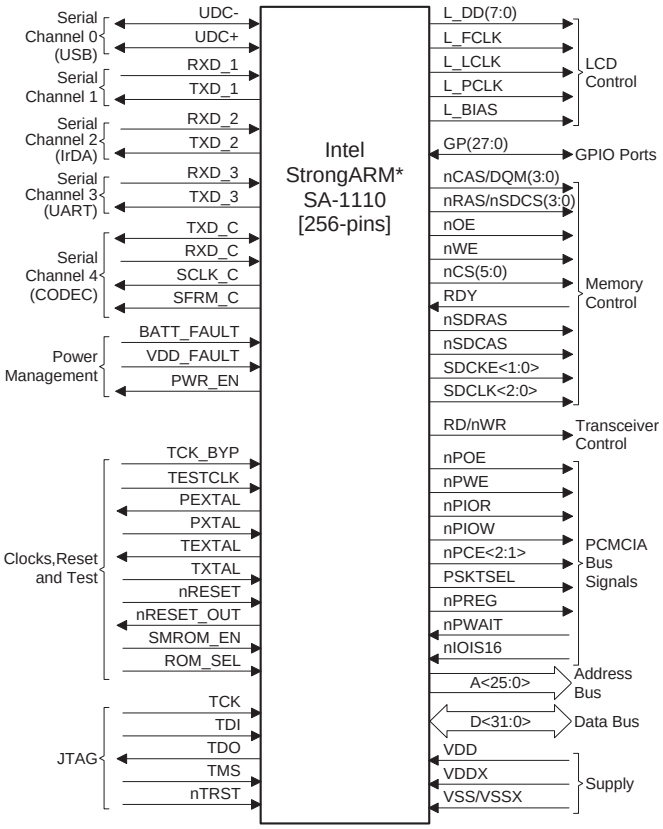
(3) SYSTEM CONFIGURATION

(3)-1. BLOCK DIAGRAM



*Other brands and names are the property of their respective owners.

(3)-2. SA-1110 FUNCTIONAL DIAGRAM



*Other brands and names are the property of their respective owners.

(4) SIGNAL DESCRIPTION

The following table describes the signals.

Key to Signal Types: n:Active low signal

IC:Input, CMOS threshold

ICOCZ:Input, CMOS threshold, output CMOS levels, tristatable

OCZ:Output, CMOS levels, tristatable

(4)-1. SIGNAL DESCRIPTION

Name	Type	Description
A 25:0	OCZ	Memory address bus. This bus signals the address requested for memory accesses. Bits 24..10 carry the 15-bit DRAM address. The static memory devices and the expansion bus receive address bits 25..0.
D 31:0	ICOCZ	Memory data bus. Bits 15..0 are used for 16-bit data busses.
nCS 5:0	OCZ	Static chip selects. These signals are chip selects to static memory devices such as ROM and Flash. They are Individually programmable in the memory configuration registers. Bits 5..3 can be used with variable latency I/O devices.
RDY	IC	Static data ready signal for nCS 5:3. This signal should be connected to the data ready output pins of variable latency I/O devices that require variable data latencies. Devices selected by nCS 5:3 can share the RDY pin if they drive it high prior to tristating and a weak external pull-up is present.
nOE	OCZ	Memory output enable. This signal should be connected to the output enables of memory devices to control their data bus drivers.
nWE	OCZ	Memory write enable. This signal should be connected to the write enables of memory devices. This signal is used in conjunction with nCAS 3:0 to perform byte writes.
nRAS 3:0/nSDCS 3:0	OCZ	DRAM RAS or SDRAM CS for banks 0 through 3. These signals should be connected to the row address strobe (RAS) pins for asynchronous DRAM or the chip select (CS) pins for SDRAM.
nCAS 3:0/DQM 3:0	OCZ	DRAM CAS or SDRAM DQM for data banks 0 through 3. These signals should be connected to the column address strobe (CAS) pins for asynchronous DRAM or the data output mask enables (DQM) for SDRAM.
nSDRAS	OCZ	SDRAM RAS. This signal should be connected to the row address strobe (RAS) pins for all banks of SDRAM.
nSDCAS	OCZ	SDRAM CAS. This signal should be connected to the column address strobe (CAS) pins for all banks of SDRAM.
SDCKE 1:0	OCZ	SDRAM and/or SMROM clock enables. SDCKE 0 should be connected to the clock enable (CKE) pins of SMROM. SDCKE 0 is asserted upon any rest (including sleep-exit) if static memory bank 0 (boot space) is configured for synchronous mask ROM (SMROM_EN = 1);otherwise it is deasserted upon reset. SDCKE 1 should be connected to the clock enable pins of SDRAM. They are deasserted (held low) during sleep. SDCKE 1 always is deasserted upon reset. The memory controller provides control register bits for deassertion of each SDCKE pin. However, SDCKE 0 cannot be deasserted via program if SMROM_EN = 1.
CDCLK 2:0	OCZ	SDRAM and/or SMROM clock. SDCLK 0 should be connected to the clock (CLK) pins of SMROM. SDCLK 1 and SDCLK 2 should be connected to the clock pins of SDRAM in bank pairs 0/1 and 2/3, respectively. They are driven by either the internal memory controller clock (CPU clock divided by 2) or the memory controller clock divided by 2 (CPU clock divided by 4). All SDCLK pins are held low during sleep mode and start running at CPU clock divide by 4 upon any reset (including sleep-exit). The memory controller provides control register bits for clock division and disable of each SDCLK pin. However, SDCLK 0 cannot be disabled via program if static memory bank 0 (boot space) is configured for synchronous mask ROM (SMROM_EN = 1).
RD/nWR	OCZ	Read/write direction control for memory and PCMCIA data bus (D 31:0). This signal is applicable to all memory bus and PCMCIA transfers. For reads (RD/nWR = 1), system-level bus transceivers or directly connected memory devices should drive D 31:0. For writes (RD/nWR = 0), the SA-1110 will drive D 31:0.
nPOE	OCZ	PCMCIA output enable. This signal is an output and is used to perform reads from memory and attribute space.
nPWE	OCZ	PCMCIA write enable. This signal is an output and is used to perform writes to memory and attribute space.

Name	Type	Description
nPIOW	OCZ	PCMCIA I/O write. This signal is an output and is used to perform write transactions to the PCMCIA I/O space.
nPIOR	OCZ	PCMCIA I/O read. This signal is an output and is used to perform read transactions from the PCMCIA I/O space.
nPCE 2:1	OCZ	PCMCIA card enable. These signals are output and are used to select a PCMCIA card. nPCE 2 enables the high-byte lane and nPCE 1 enables the low-byte lane.
nIOIS16	IC	I/O Select 16. This signal is an input and is an acknowledgment from the PCMCIA card that it can perform 16-bit I/O data transfers.
nPWAIT	IC	PCMCIA wait. This signal is an input and is driven low by the PCMCIA card to extend the duration of transfers to/from the SA-1110.
PSKTSEL	OCZ	PCMCIA socket select. This signal is an output and used by external steering logic to route control, address, and data signals to one of the PCMCIA sockets. When PSKTSEL is low, socket zero is selected. When PSKTSEL is high, socket one is selected. This signal has the same timing as the address lines.
nPREG	OCZ	PCMCIA register select. This signal is an output and indicates that, on a memory transaction, the target address is attribute space. This signal has the same timing as address.
L_DD 7:0	OCZ	LCD controller display data.
L_FCLK	OCZ	LCD frame clock.
L_LCLK	OCZ	LCD line clock.
L_PCLK	OCZ	LCD pixel clock.
L_BIAS	OCZ	LCD ac bias drive.
TXD_C	OCZ	CODEC transmit.
RXD_C	IC	CODEC receive.
SCLK_C	OCZ	CODEC clock.
SFRM_C	OCZ	CODEC frame signal
UDC+	ICOCZ	Serial port zero bidirectional, differential signalling pin (UDC).
UDC	ICOCZ	Serial port zero bidirectional, differential signalling pin (UDC).
TXD_1	OCZ	Serial port one transmit pin (UART).
RXD_1	IC	Serial port one receive pin (UART).
TXD_2	OCZ	Serial port two transmit pin (IrDA).
RXD_2	IC	Serial port two receive pin (IrDA).
TXD_3	OCZ	Serial port three transmit pin (UART).
RXD_3	IC	Serial port three receive pin (UART).
GP 27:0	ICOCZ	General-purpose input output.
SMROM_EN	IC	Synchronous mask ROM (SMROM) enable. This pin is used to determine if the boot ROM (static memory bank 0) is asynchronous or synchronous. If asynchronous, boot ROM is selected (SMROM_EN = 0) and its width is determined by the state of the ROM_SEL pin. SMROM is supported only on 32-bit data busses.
ROM_SEL	IC	ROM select. This pin is used to configure the ROM width. It is either grounded or pulled high. If ROM_SEL is grounded, the ROM width is 16 bits. If ROM_SEL is pulled up, the ROM width is 32 bits.
PXTAL	IC	Input connection for 3.686-MHz crystal (non-CMOS threshold).
PEXTAL	OCZ	Output connection for 3.686-MHz crystal (non-CMOS level).
TXTAL	IC	Input connection for 32.768-kHz crystal (non-CMOS threshold).
TEXTAL	OCZ	Output connection for 32.768-kHz crystal (non-CMOS level).
PWR_EN	OCZ	Power enable. Active high. PWR_EN enables the external VDD power supply. Deasserting it signals the power supply that the system is going into sleep mode and that the VDD power supply should be removed.
BATT_FAULT	IC	Battery fault. Signals the SA-1110 that the main power source is going away (battery is low or has been removed from the system). The assertion of BATT_FAULT causes the SA-1110 to enter sleep mode. The SA-1110 will not recognize a wake-up event while this signal is asserted.
VDD_FAULT	IC	VDD fault. Signals the SA-1110 that the main power supply is going out of regulation (shorted card is inserted). VDD_FAULT will cause the SA-1110 to enter sleep mode. VDD_FAULT is ignored after a wake-up event untill the power supply timer completes (approximately 10ms).
nRESET	IC	Hard reset. This active low signal is a level-sensitive input used to start the processor from a known address. A low level will cause the current instruction to terminate abnormally, and the on-chip caches, MMU, and write buffer to be disabled. When nRESET is driven high, the processor will restart from address 0. nRESET must remain low until the power supply is stable and the internal 3.686-MHz oscillator has come up to speed. While nRESET is low, the processor will perform idle cycles.

Name	Type	Description
nRESET_OUT	OCZ	Reset out. This signal is asserted when nRESET is asserted and deasserts when the processor has completed resetting. nRESET_OUT is also asserted for "soft" reset events (sleep and watchdog).
nTRST	IC	Test interface reset. Note this pin has an internal pull-down resistor and must be driven high to enable the JTAG circuitry. If left unconnected, this pin is pulled low and disables JTAG operation.
TDI	IC	JTAG test interface data input. Note this pin has an internal pull-up resistor.
TDO	OCZ	JTAG test interface data output. Note this pin does not have an internal pull-up resistor.
TMS	IC	JTAG test interface mode select. Note this pin has an internal pull-up resistor.
TCK	IC	JTAG test interface reference clock. This times all the transfers on the JTAG test interface. Note this pin has an internal pull-down resistor.
TCK_BYP	IC	Test clock PLL bypass. When TCK_BYP is high, the TESTCLK is used as the core clock in place of the PLL clock; when low, the internal PLL output is used. This signal has no relation to the JTAG TCK pin.
TESTCLK	IC	Test clock . TESTCLK is used to provide the core clock when TCK_BYP is high. It should be tied low if TCK_BYP is low. This pin should be used for test purposes only. An end user should ground this pin.
VDD	–	Positive supply for the core. Nine pins are allocated to this supply; eight pins are labeled VDD. The ninth pin, labeled VDDP is dedicated to the PLL supply and should have its own dedicated decoupling capacitor. Also, it should be tied directly to the VDD power plane with the other eight VDD pins.
VDDX	–	Positive supply for the pins. For a count of VDDX pins. All of the pins allocated to VDDX (labeled VDDX1, VDDX2, and VDDX3) should be tied directly to the VDDX power plane. VDDX3 should have its own dedicated decoupling capacitor.
VSS	–	Ground supply. Nine pins are allocated to VSS, including one for the PLL.
VSSX	–	Ground supply for the I/O pins. "Package and Pinout", for a count of VSSX pins.

2-2. ANALOG FRONT END LSI (TC35143AF)

(1) OUTLINE

TC35143AF is an analog front end LSI suitable for personal digital assistants (PDA) including HPC. It consists of a V.34 modem tele-phone line interface, sound interface compatible with the handsfree / handset system, and touch screen interface. The communication with the host processor is performed through the SIB (Serial Interface Bus). The LSI is connectable to a master processor with an SIB interface. Clocks used inside the TC35143AF are generated from the serial transfer clocks of the SIB interface. There is no need for any clock oscillator. Sampling data, control signals and status of each interface block is communicated with the host processor through the SIB interface.

(2) FEATURES

(2)-1. TELEPHONE LINE INTERFACE

- 16-bit ADC/DAC
- Programmable input amplifier gain (2-stage, in steps of 6dB)
- Full differential telephone line interface
- Analog echo canceller is incorporated
- Programmable sampling frequency (3-stage : 7.2 kHz, 8 kHz, 9.6 kHz)

(2)-2. SOUND INTERFACE

- 14-bit ADC/DAC
- 2 mike input lines, 2 speaker output lines (supports handsfree, handset system)
- Power On/Off function for each block
- Mike input mute switch, speaker input mute switch
- Programmable mike amplifier gain (2 types: 15 stages in steps of 1.5dB and 4 stages in steps of 6dB)
- Programmable speaker output level attenuator (8 stages in steps of 3dB)
- Programmable sampling frequency (4 stages in steps of 8 kHz, about 11.03 kHz, 16 kHz, about 22.05 kHz)

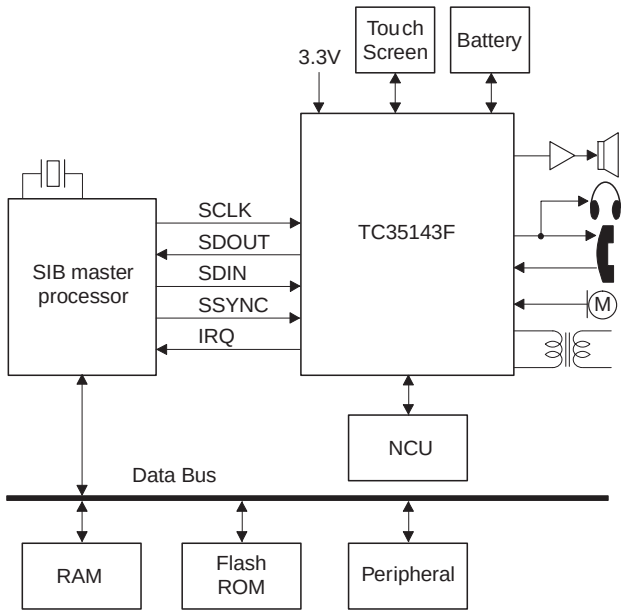
(2)-3. TOUCH SCREEN INTERFACE

- Voltage measurement 10-bit ADC
- Touch starting mode from stand-by state
- Plate applied voltage generation circuit
- General-purpose analog input port (4 inputs)

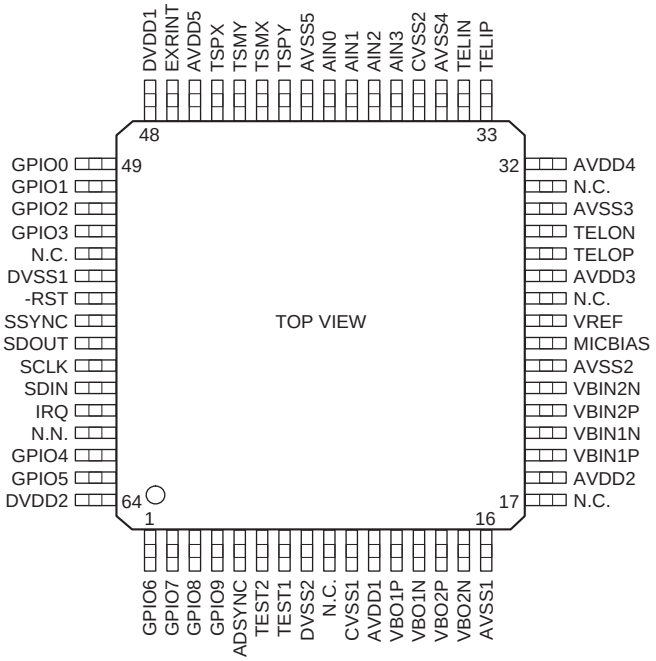
(2)-4. OTHERS

- Interrupt output port (programmable interrupt factor setting function)
- Multichip connection through SIB interface (SIB clock input fixed to 9.216 MHz)
- General-purpose I/O port (10 ch)
- +3.3V battery power supply
- 64-pin QFP package

(3) SYSTEM BLOCK DIAGRAM



(4) PIN DESCRIPTION



(5) PIN FUNCTION

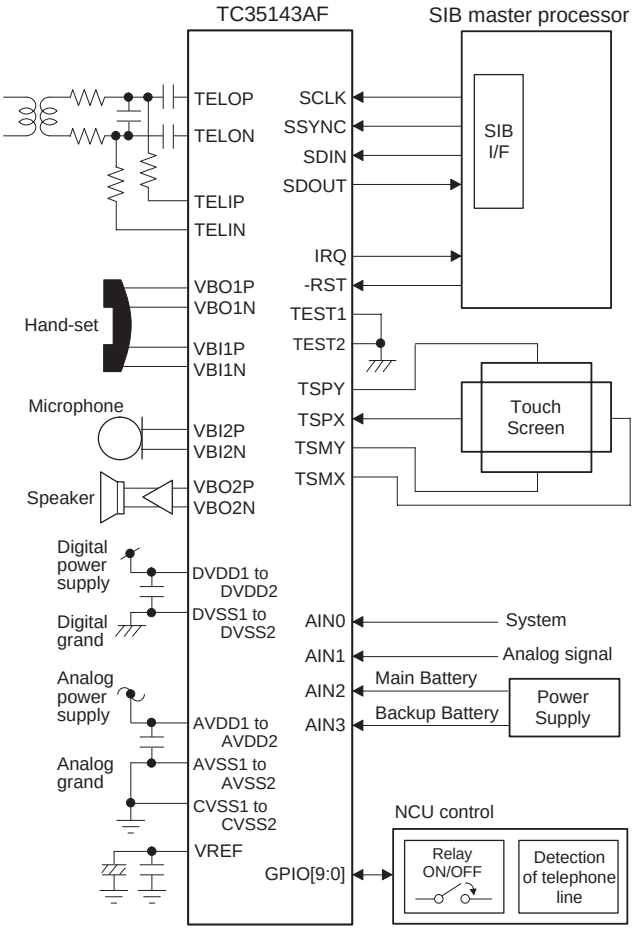
Symbol	Pin No.	A/D/P	I/O	DEF	Group	Deption
SCLK	58	D	I	–	HOST	Serial data transfer clock. Serial data is transferred synchronizing with this clock. SCLK is used as the master clock for TC35143AF. The specification of SCLK is 9.216 MHz, with duty ratio 50%. Connect to the clock output of SIB master chip.
SSYNC	56	D	I		HOST	This signal provides synchronization for serial data frames. 72kHz clock. 1 frame consists of 128 bits of serial data. Connect to the synchronizing signal output of SIB master chip.
SDIN	59	D	I		HOST	Serial input data terminal. Serial data input through the SDIN terminal is latched inside at the falling edge of SCLK. Connect to the data output of SIB master chip.
SDOUT	57	D	O	HZ	HOST	Serial output data terminal. Serial data output through SDOUT terminal is output, synchronizing with the rising edge of SCLK. Connect to the data input of SIB masterchip.
IRQ	60	D	O	L	HOST	Interrupt output terminal. Interrupt factors output from the control resistor to this terminal are set. The signal level at the time of interrupt is active high.
RST	55	D	I	–	HOST	System reset. This signal is active low.
TSPX	45	A	I/O	HZ(IN)	TSC	Interface terminal for touch screen X plate. Open when not in use.
TSMX	43	A	I/O	HZ(IN)	TSC	Interface terminal for touch screen X place. Open when not in use.
TSPY	42	A	I/O	HZ(IN)	TSC	Interface terminal for touch screen Y plate. Open when not in use.
TSMY	44	A	I/O	HZ(IN)	TSC	Interface terminal for touch screen Y plate. Open when not in use.
AIN0	40	A	I	–	ADC	ADC input
AIN1	39	A	I	–	ADC	ADC input
AIN2	38	A	I	–	ADC	ADC input
AIN3	37	A	I	–	ADC	ADC input
ADSYNC	5	D	I	–	ADC	Synchronizing clock input terminal when putting 10-bit ADC in the external clock synchronizing mode. ADC starts conversion synchronizing with the edge of ADSYNC.Pull down when not in use.
EXRINT	47	A	I	–	TSC	Terminal to which external resistance is connected, for adjusting detection sensitivity in touch detection mode. Connect a resistance of more than 16kΩ between AVDD5.
TELOP	28	A	O	HZ	TEL	Positive polarity output terminal for telephone line CODEC
TELON	29	A	O	HZ	TEL	Negative polarity output terminal for telephone line CODEC
TELIP	33	A	I	–	TEL	Positive polarity input terminal for telephone line CODEC. Open when not in use.
TELIN	34	A	I	–	TEL	Negative polarity input terminal for telephone line CODEC. Open when not in use.
VBO1P	12	A	O	HZ	VB	Positive polarity output terminal 1 for sound CODEC. It is used for the handset speaker.
VBO1N	13	A	O	HZ	VB	Negative polarity output terminal 1 for sound CODEC. It is used for the handset speaker.

Symbol	Pin No.	A/D/P	I/O	DEF	Group	Deption
VBO2P	14	A	O	HZ	VB	Positive polarity output terminal 2 for sound CODEC. It is used for the external speaker.
VBO2N	15	A	O	HZ	VB	Negative polarity output terminal 2 for sound CODEC. It is used for the external speaker.
VB1N1P	19	A	I	–	VB	Positive polarity input terminal 1 for sound CODEC. It is used for the hand mike. Open when not in use.
VBIN1N	20	A	I	–	VB	Negative polarity input terminal 1 for sound CODEC. It is used for the hand mike. Open when not in use.
VBIN2P	21	A	I	–	VB	Positive polarity input terminal 2 for sound CODEC. It is used for the external mike. Open when not in use.
VBIN2N	22	A	I	–	VB	Negative polarity input terminal 2 for sound CODEC. It is used for the external mike. Open when not in use.
MICBIAS	24	A	O	HZ	VB	This is a power supply terminal for an electret condenser mphone. Insert a 2-kΩ resistance and more than 10μF electrolytic capacitor in series between this pin and the analog GND.
GPIO0	49	D	I/O	HZ(IN)	GPIO	These are general-purpose I/O ports. The selection of input and output and the output level are set by the control resistor. After resetting, the ports are put in the input mode as a default state. Pull down when not in use.
GPIO1	50	D	I/O	HZ(IN)	GPIO	GPIO
GPIO2	51	D	I/O	HZ(IN)	GPIO	GPIO
GPIO3	52	D	I/O	HZ(IN)	GPIO	GPIO
GPIO4	62	D	I/O	HZ(IN)	GPIO	GPIO
GPIO5	63	D	I/O	HZ(IN)	GPIO	GPIO
GPIO6	1	D	I/O	HZ(IN)	GPIO	GPIO
GPIO7	2	D	I/O	HZ(IN)	GPIO	GPIO
GPIO8	3	D	I/O	HZ(IN)	GPIO	GPIO
GPIO9	4	D	I/O	HZ(IN)	GPIO	GPIO
TEST1	7	D	I	–	ETC	Test pin. Fix to GND.
TEST2	6	D	I	–	ETC	Test pin. Fix to GND.
VREF	25	A	I/O	HZ (OUT)	ETC	This pin is an internal analog reference voltage. Insert an electrolytic capacitor of more than 10μF between this pin and analog GND. The attributes of input and output, are determined by resistor setting.
DVDD1	48	P	–	–	POW	This pin is a digital power supply. Fix to +3.3V. Insert a 0.1μF laminated ceramic capacitor between this pin and the digital VSS of the same number. Insert the capacitor as close to the pin as possible.
DVDD2	64	P	–	–	POW	
AVDD1	11	P	–	–	POW	This pin is an analog power supply. Fix to +3.3 V. Insert a 0.1μF laminated ceramic capacitor between this pin and the analog VSS of the same number. Insert the capacitor as close to the pin as possible.
AVDD2	18	P	–	–	POW	
AVDD3	27	P	–	–	POW	
AVDD4	32	P	–	–	POW	
AVDD5	46	P	–	–	POW	
DVSS1	54	P	–	–	POW	Connect this pin to the digital GND. The pattern must be designed so that this pin is separated from the analog GND.
DVSS2	8	P	–	–	POW	
AVSS1	16	P	–	–	POW	Connect this pin to the analog GND. The pattern must be designed so that this pin is separated from the digital GND.
AVSS2	23	P	–	–	POW	
AVSS3	30	P	–	–	POW	
AVSS4	35	P	–	–	POW	
AVSS5	41	P	–	–	POW	
CVSS1	10	P	–	–	POW	This is a common GND for the analog and digital sections. Connect this pin to theanalog GND.
CVSS2	36	P	–	–	POW	
N.C.	9, 17, 26, 31, 53, 61	–	–	–	–	Non-connection pin. Make is open.

Note:

- A/D/P mean an Analog terminal, Digital terminal, and Power terminal.
- DEF means reset state. H/L stand for output levels. Hz means high impedance and IN means input state (high impedance).
- Group categories are as follows :
  HOST-Host interface, TSC-Touch screen interface, TEL-Telecom CODE, VB-Voice band CODEC, ETC-The other, POW-power supply.

(6) HARDWARE INTERFACE

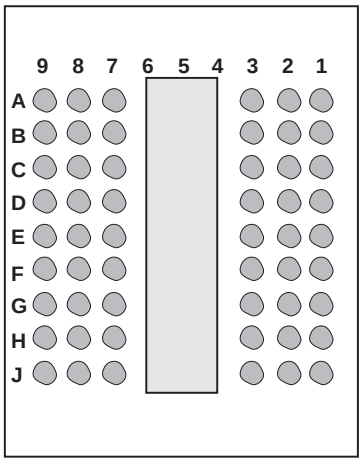


2-3. 256Mbit SDRAM (K4S561633C-RL75)

(1) DESCRIPTION

The K4S561633C is 268, 435, 456 bits synchronous high data rate Dynamic RAM organized as 4 x 4, 196, 304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

(2) PIN CONFIGURATION



54Ball (6 x 9) CSP						
	1	2	3	7	8	9
A	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ	VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ	VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ	VSSQ	DQ6	DQ5
E	DQ8	NC	VSS	VDD	LDQM	DQ7
F	UDQM	CLK	CKE	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	A12	A11	A9	BA0	BA1	$\overline{CS}$
H	A8	A7	A6	A0	A1	A10
J	VSS	A5	A4	A3	A2	VDD

(3) PIN FUNCTION

Pin Name	Pin Function
CLK	System Clock
$\overline{CS}$	Chip Select
CKE	Clock Enable
A0~A12	Address
BA0~BA1	Bank Select Address
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
L (U) DQM	Data Input/Output Mask
DQ0~15	Data Input/Output
VDD/VSS	Power Supply/Ground
VDDQ/VSSQ	Data Output Power/Ground

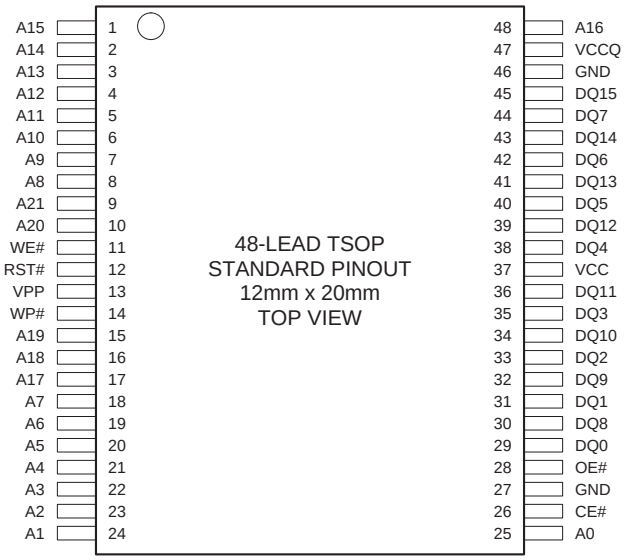
2-4. 64Mbit FLASH MEMORY (LF28F640BX)

(1) DESCRIPTION

The LH28F640BX series page-mode dual-work flash memory has the following features.

- Dual work function
- Settable partition configuration
- Page buffer program
- Data protection function for each block and full-block lock function at power-on.
- 8-word OTP (One Time Program) block
- Low power consumption
- Parameter block configuration

(2) PIN CONFIGURATION



(3) PIN NAMES

Symbol	Type	Name and function
A0-A21	Input	Address input: Address input pin 64M: A0-A21
DQ0-DQ15	Input/ Output	Data I/O: This pin outputs data that is written to CUI (Command User Interface), command input, memory array, status register, query code, ID code, and device configuration code read data. When the chip is not selected or output is disabled, the pin is at high impedance (High Z). Data is erased or latched internally while a program is running.
CE#	Input	Chip enable: This pin activates device control logic, input buffer, decoder and sense amplifier. When CE# is VIH, device is not selected and power turns to stand-by level.
RST#	Input	Reset: When RST# is VIL, the inside of device is automatically reset to prohibit erasure and running of the program, thus protecting data. When RST# is VIH, device is set to usual operation mode. After power is turned on, or after power is restored from the reset mode, device is automatically set to a synchronous array read mode. when power is turned on, RST# needs to be set to VIL.
OE#	Input	Output enable: This pin controls the output terminal of device in reading.
WE#	Input	Write enable: This pin controls writing to CUI and memory array. The address and data are latched at the leading edge of CE# or WE# whichever comes first.
WP#	Input	Write protect: When WP# is VIL, The release of lock bit in the block to which lock-down bit is set is prohibited. For blocks to which either lock bit or lock-down bit is not set, erasure or program operation can be performed. Lock-down bit can be disabled by putting WP# in VIH.
VPP	Input	Power supply voltage detection pin: VPP is not a power supply pin. When VPP VPPLK, it is not possible to execute block erasure, full-chip erasure, (page buffer) program or OTP program. Do not try to execute such operations. High-speed erasure and high-speed program operation can be executed by applying a voltage of 12V ± 0.3 V to VPP, and at this time, VPP acts as a power supply pin. If VPP voltage is used at 12V ± 0.3V during erasure or the running of a program, the number of rewrites per block is up to 1000. If 12V ± 0.3V is applied to VPP pin, it is required to set up to 80 hours in accumulation. If more than 12V is applied to VPP, there is a possibility of reducing the number of rewrites or irreversible destruction.
VCC	Supply	Device power supply (see delivery specification): When VCCVLKO, writing to flash memory is prohibited. If the system is used at an invalid VCC voltage (see DC characteristics), malfunction might result. Do not use the system at such a state.
VCCQ	Supply	I/O power supply (see delivery specification); Power supply for I/O pin
GND	Supply	Ground: All ground pins need to be connected.
NC		This pin is not connected to the internal circuit. It may be used in open state.

2-5. GATE ARRAY SPECIFICATION

(1) GENERAL DESCRIPTION

The LOCOMO-QFP15-128pin G/A (SLA5075H) is a gate array developed for the SL-5500.

The outlines of built-in functions are described below.

(2) FUNCTION DESCRIPTION

(2)-1. BOOT SWITCHING, MCS DECODER [memc]

(2)-1-1. Outline

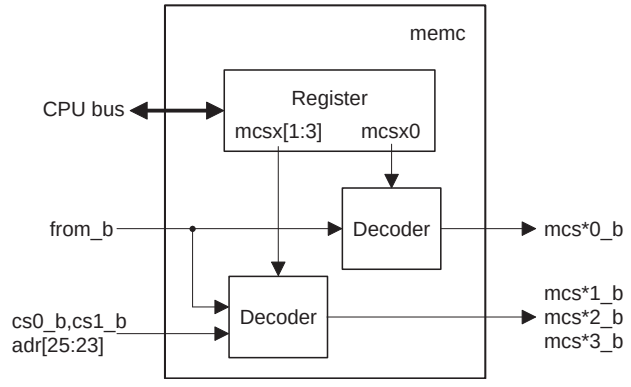
This module divides the area of chip select signal connected to cs0_b and cs1_b pins into mos00_b, mos01_b, mos02_b, mos03_b, mos10_b, mos11_b, mos12_b, and mos13_b according to the capacity of memory to be connected.

In addition, the module detects the connection of FROM with from_b. If FROM is inserted, os0_b is replaced with os1_b and decoded to start from memory connected to os1_b.

This module is not affected by the state of pwren or battfault.

(2)-1-2. Block diagram

Here is a block diagram of this module.



(2)-2. SPI I/F

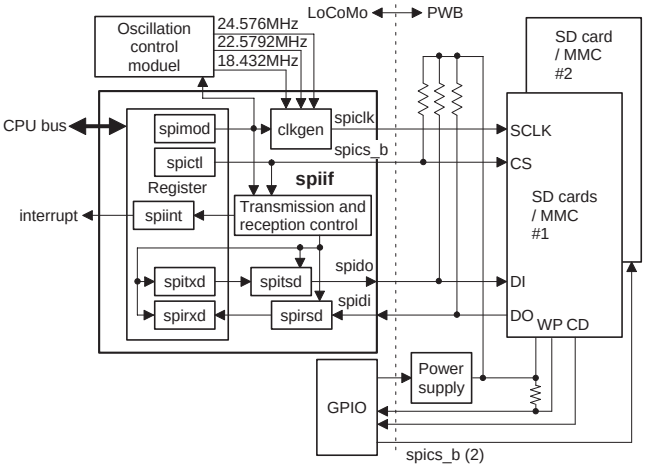
(2)-2-1. Outline

This module interfaces SD card and MMC in the SPI mode and has the following features:

- Capable of interfacing multiple SD cards and MMCs. However, since there is a single spics_b, control is required using GP10 and others.
- spidi needs a pull-up resistance outside.
- Clock synchronous type serial port and data length can be selected between 8 and 16 bits.
  The data length set forth in this specification is called unit.
- Double buffers for transmission and reception (no FIFO) make it possible to perform transmission and reception continuously.
- In transmission and reception, it is possible to select whether data alignment (transmission and reception synchronized in the unit of "unit") is carried out or not can be selected.
- Clock frequency can be selected from among 15 bands (24.576MHz - 2.304MHz and 384 kHz - 288 KHz).
- There are 4 interrupts including reception data read enable, transmission data write enable, transmission end, and reception end. They can be separately allowed or prohibited.
- When this module is not in use, clock can be stopped to reduce power consumption.
- MSB/LSB first can be selected.
- Transmission and reception bit can be freely reversed.
- Test can be performed by looping back the status of spido to spidi, without suing any jig.
- The timing between transmission and reception data and clock can be set. The status of spido can be set after data is transmitted or received or while data is only received.
- This module is not affected by pwren, but when battfault is at L, it is reset.

(2)-2-2. Block diagram

Here is a block diagram of this module.

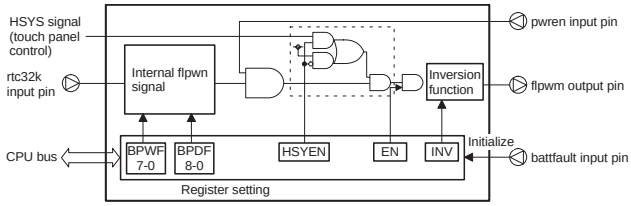


(2)-3. FRONT LIGHT CONTROL

(2)-3-1. Outline

- This module outputs the pulse modulation output signal for controlling the front light DUTY. It has the following features:
- Front light DUTY control pulse modulation output (Cycle and DUTY can be changed)
- Fixed output at PWREN and internal Enbit
- Inverted output at INVbit is possible
- When BATTFAULT pin input level is Low, the register of this module is initialized.

(2)-3-2. Block diagram



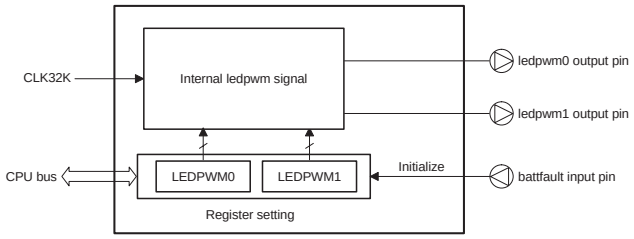
(2)-4. LED CONTROLLER

(2)-4-1. Outline

This module outputs the pulse modulation output signal for LED light emission to the LEDPWM0, 1 pins. It has the following features:

- Outputs the pulse modulation output signal for LED light emission to the LEDPWM0, 1 pins. Cycle and DUTY can be separately changed.
- When the BATTFAULT pin input level is at Low, the register of this module is initialized.

(2)-4-2. Block diagram



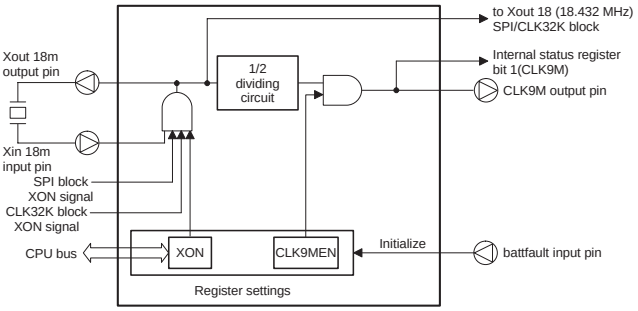
(2)-5. TOSHIBA ANALOG FRONT END LSI OSCILLATION CIRCUIT

(2)-5-1. Outline

This module outputs 9.216MHz clock signal to Toshiba analog end LSI (TC35143AF). It has the following features:

- Outputs 9.216MHz clock signal from LCK9M pin.
- The registers of this module are initialized when BATTFAULT pin input level is at LOW.
- This module is not affected by pwren pin input.
- Capable of monitoring the same signal as that from CLK9M pin using the status register (04h) bit1 (clk9m).

(2)-5-2. Block diagram (Here is a circuit image.)

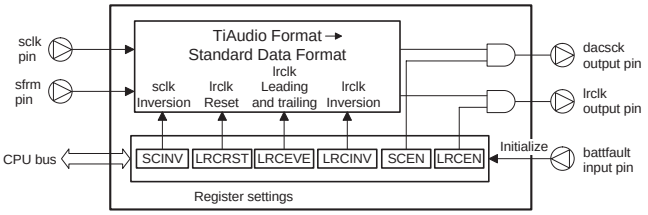


(2)-6. PCM AUDIO INTERFACE

(2)-6-1. Outline

- The registers of this module are initialized when the BATTFAULT pin input level is at LOW.
- This module is not affected by pwren pin input.
- Converts audio data from Ti Audio Format generated by the SSP of the CPU into Standard Data Format.

(2)-6-2. Block diagram

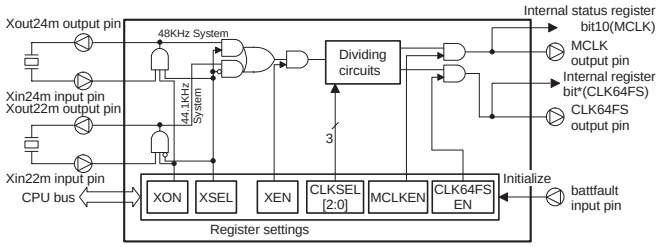


(2)-7. AUDIO CLOCK

(2)-7-1. Outline

- The registers of this module are initialized when the BATTFAULT pin input level is at LOW.
- When pwren pin input level is at LOW, the output of mclk and clk64fs pins becomes LOW regardless of the register settings.
- Capable of monitoring the same signal as those from MCLK / CLK64FS pins using the status register (04h) bit 0 (MCLK) / bit0 (CLK64FS).

(2)-7-2. Block diagram



(2)-8. GENERAL-PURPOSE 8-bit 2ch DAC CONTROL SIGNAL

(2)-8-1. Outline

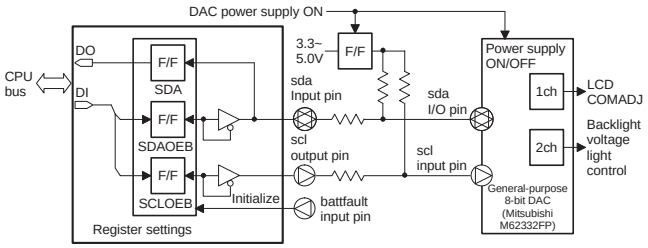
- The registers of this module are initialized when BATTFAULT pin input level is at LOW.
- The operation of this module does not depend upon the input level of the pwren pin.

Buffer of each pin:

SCL OUTPUT N-CH Open Drain 5-V withstand voltage, 2mA
SDA INPUT 5-V withstand voltage, 2mA (not a feed-through current prevention

buffer)

(2)-8-2. Block diagram

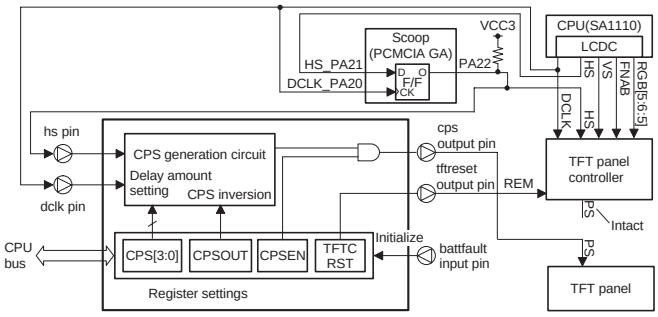


(2)-9. TFT-RELATED SIGNAL

(2)-9-1. Outline

- The registers of this module are initialized when the BATTFAULT pin input lever is at LOW.
- The operation of this module does not depend upon pwren pin input level.

(2)-9-2. Block diagram

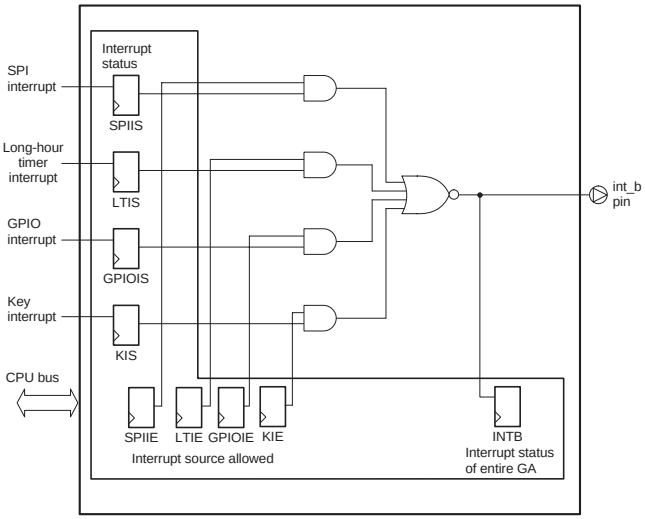


(2)-10. INTERRUPT CONTROLLER

(2)-10-1. Outline

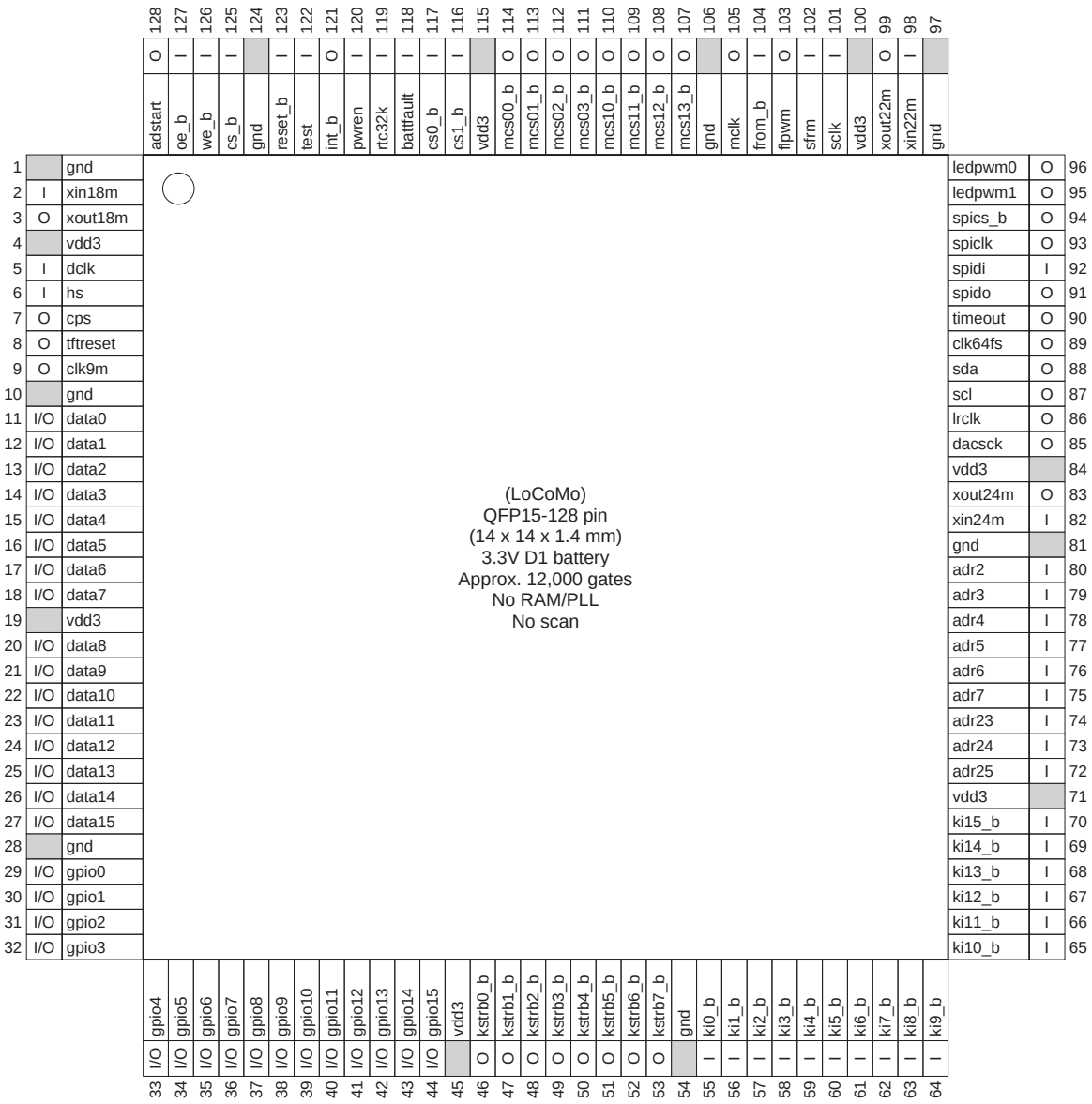
- The registers of this module are initialized when batterfault pin input level is LOW.
- The operation of this module does not depend upon pwren pin input level.

(2)-10-2. Block diagram (Here is a circuit image.)



(3) PIN CONFIGURATION

LoCoMo 128 pin diagram (SLA 50000 series (SLA5075H))



128	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97
O	I	I	I		I	I	O	I	I	I	I	I		O	O	O	O	O	O	O	O		O	I	O	I	I		O	I	
adstart	oe_b	we_b	cs_b	gnd	reset_b	test	int_b	pwren	rtc32k	battfault	cs0_b	cs1_b	vdd3	mcs00_b	mcs01_b	mcs02_b	mcs03_b	mcs10_b	mcs11_b	mcs12_b	mcs13_b	gnd	mclk	from_b	flpwm	sfrm	sclk	vdd3	xout22m	xin22m	gnd

33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	O	O	O	O	O	O	O	O		I	I	I	I	I	I	I	I	I	I
gpio4	gpio5	gpio6	gpio7	gpio8	gpio9	gpio10	gpio11	gpio12	gpio13	gpio14	gpio15	vdd3	kstrb0_b	kstrb1_b	kstrb2_b	kstrb3_b	kstrb4_b	kstrb5_b	kstrb6_b	kstrb7_b	gnd	ki0_b	ki1_b	ki2_b	ki3_b	ki4_b	ki5_b	ki6_b	ki7_b	ki8_b	ki9_b

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	I	O		I	I	O	O	O		I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O		I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O		I/O	I/O	I/O	I/O
gnd	xin18m	xout18m	vdd3	dclk	hs	cps	tftreset	clk9m	gnd	data0	data1	data2	data3	data4	data5	data6	data7	vdd3	data8	data9	data10	data11	data12	data13	data14	data15	gnd	gpio0	gpio1	gpio2	gpio3

96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65
O	O	O	O	I	O	O	O	O	O	O	O		O	I		I	I	I	I	I	I	I	I	I		I	I	I	I	I	I
ledpwm0	ledpwm1	spics_b	spiclk	spidi	spido	timeout	clk64fs	sda	scl	lrclk	dacsck	vdd3	xout24m	xin24m	gnd	adr2	adr3	adr4	adr5	adr6	adr7	adr23	adr24	adr25	vdd3	ki15_b	ki14_b	ki13_b	ki12_b	ki11_b	ki10_b

Note 1: Oscillation frequency
Nos. 2 and 3 pins (xin18m, xout 18m): 18.432MHz (ceramic oscillator)
Nos. 82 and 83 pins (xin24m, xout24m):24.567MHz (ceramic oscillator)
Nos. 98 and 99 pins (xin22m, xout22m):22.5792MHz (ceramic oscillator) Correct matching is required.

Note 2: Nos. 11-27 pins (data [15:0] data bus): Bus cycle 30MHz
Nos. 72-82 pins (adr [7:2], [25:23] address bus): Bus cycle 30MHz

(4) PIN FUNCTION

(4)-1. PIN DESCRIPTION BY FUNCTION (128-PIN SPECIFICATION)

Function	Pin name	Pin No.	Q'ty	I/O	Buffer	Description	Connected to
SA1110 interface (Variable Latency I/O)	BATTFAULT		1	IN	IBC	Battery voltage detection input	Detection circuit
	PWREN		1	IN	IBC	CPU status input (L: HALT, H: Operate)	
	RESET_B		1	IN	IBH	Reset input	CPU (SA1110)
	RTC32K		1	IN	IBO	RTC 32 kHz clock signal input	CPU (SA1110)
	CS_B		1	IN	IBO	Chip selection signal for GA	CPU (SA1110)
	WE_B		1	IN	IBO	Write enable signal for GA	CPU (SA1110)
	OE_B		1	IN	IBO	Output enable signal for GA	CPU (SA1110)
	ADR[25:23]		3	IN	IBO	Address bus	CPU (SA1110)
	ADR[7:2]		6	IN	IBO	Address bus	CPU (SA1110)
	DATA[15:0]		16	IN/OUT	BA2T	Data bus	CPU (SA1110)
	Subtotal		32				
Interrupt control	INT_B		1	OUT	OB1T	INT (including interrupt key) output signal	CPU (SA1110 interrupt)
BOOT drive switching circuit and decode	CS[1:0]_B		2	IN	IBO	CS signal for FROM/MROM signal	CPU (SA1110)
	MCS0[3:0]_B		4	OUT	OB1T	MCS signal 0 for FROM/MROM decode signal	FROM/MROM
	MCS1[3:0]_B		4	OUT	OB1T	MCS signal 1 for FROM/MROM decode signal	FROM/MROM
	FROM_B		1	IN	IBOP2	FROM_Board detection pin	FROM/MROM
	Subtotal		11				
Key port circuit	KSTRB[7:0]		8	OUT	TB1HT	Key strobe signal	KEY_BOARD
	KI_B[15:0]		16	IN	IBH	Key input signal (external pull-up resistance is required)	KEY_BOARD
	Subtotal		24				
Serial output circuit for general-purpose 8-bit 2ch DAC control	SCL		1	OUT	OD1T	Serial clock signal	DAC
	SDA		1	IN/OUT	BG1	Serial data	DAC
	Subtotal		2				
TFT_C reset	TFTRESET		1	OUT	OB1T	TFT_C reset signal	
TFT PS control	CPS		1	OUT	OB1T	TFT power save CPS output signal	TFT panel
AD_START output circuit for tablet control	ADSTART		1	OUT	IBO	Tablet incorporation START signal	Toshiba TC35143AF
	HS		1	IN	IBO	LCD horizontal synchronous signal	CPU (SA1110-I, CDC)
	DCLK		1	IN	IBO	LCD data transfer clock signal	CPU (SA1110-I, CDC)
	Subtotal		3				
PWM output port	TIMEOUT		1	OUT	OB2T	Battery charger protection timer	Charger circuit
	LEDPWM0		1	OUT	OB2T	For charger indicator	Charger circuit
	LEDPWM1		1	OUT	OB2T	For communication error blinking	Charger circuit
	FLPWM		1	OUT	OB1T	F/L Duty light control signal (0-100%) output	F/L inverter circuit
	Subtotal		4				
Audio MCLK/SCK32 output port	XIN22M		1	IN	LIN	44.1 KHz system base clock input (22.5792 MHz)	Oscillation circuit 1 (OSC4C)
	XOUT22M		1	OUT	LOT	44.1 KHz system base clock output (22.5792 MHz)	Oscillation circuit 1 (OSC4C)
	XIN24M		1	IN	LIN	48 KHz system base clock input (MHz)	Oscillation circuit 2 (OSC4C)
	XOUT24M		1	OUT	LOT	48 KHz system base clock output (22.5792 MHz)	Oscillation circuit 2 (OSC4C)
	CLK64FS		1	OUT	OB2T	Audio 64 fs output (SCLK x2)	CPU (GPI0)
	MCLK		1	OUT	OB2T	Audio MCLK clock output	Audio DAC
	Subtotal		6				

Function	Pin name	Pin No.	Q'ty	I/O	Buffer	Description	Connected to
PCM audio TIAudo output-SDF conversion circuit	SFRM		1	IN	IBO	Audio serial data start signal	CPU (SA1110)
	LRCLK		1	OUT	OB1T	Audio serial data right and left identification signal	Audio stereo DAC
	SCLK		1	IN	IBO	Audio serial data clock signal	CPU (SA1110)
	DACSCK		1	OUT	OB1T	Audio serial clock-SCLK inversion	Audio stereo DAC
	Subtotal		4				
SD_CARD SPI control circuit	SPICS_B		1	OUT	TB1T	SD_CARD CS signal	SD_CARD connector
	SPICLK		1	OUT	TB2T	SD_CARD clock signal	SD_CARD connector
	SPIDI		1	IN	IBO	SD_CARD data input signal	SD_CARD connector
	SPIDO		1	OUT	TB2T	SD_CARD data output signal	SD_CARD connector
	Subtotal		4				
SD_CARD/ TC35143 AF clock output	XIN18M		1	IN	LIN	SD_CARD/Toshiba TC35143AF base clock signal input (18.432 MHz)	Oscillation circuit (OSC4C)
	XOUT18M		1	IN	LOT	SD_CARD/Toshiba TC35143AF base clock signal input	Oscillation circuit (OSC4C)
	CLK9M		1	OUT	OB2T	Clock signal output (9.216 MHz)	Toshiba TC35143AF, CPU
	Subtotal		3				
GPIO port	GPIO[15, 12:3, 0]		16	I/O	BA1T	General-purpose I/O port (CMOS input + Feed-through current prevention type)	
	GPIO[14:13, 2:1]		4	I/O	BH1T	General-purpose I/O port (Schmidt input)	
TEST circuit	TEST		1	IN	ITST1	Test mode selection signal input	–
Power supply (3.3 V)	VDD3		7				
	GND		8				
TOTAL_PIN			128	QFP15 (14 x 14 x 1.4mm)			

<Description buffers>

IBC : Input buffer

IBH : Schmidt trigger input buffer

IBO : OR type gated input buffer

IBOP2 : OR type gated input buffer + 100 K pull-up

OB1T : Output buffer (IOL=2mA, with test function)

OB2T : Output buffer IOL=6mA, with test function)

TB1HT : 3-state output buffer with buss hold circuit (IOL=2mA, with test function)

OD1T : Open drain output buffer (IOL=2mA, with test function)

TB1T : Try state output buffer (IOL=2mA, with test function)

TB2T : Try state output buffer (IOL=6mA, with test function)

BG1 : 5-V withstand voltage output buffer (IOL=2mA, with test function)

BH1T : Schmidt trigger I/O buffer (IOL=2mA, with test function)

BA1T : AND type gated I/O buffer (IOL=2mA, with test function)

BA2T : AND type gated I/O buffer (IOL=6mA, with test function)

LIN : TRANSPARENT input buffer (for clock oscillation)

LOT : TRANSPARENT output buffer (for clock oscillation)

ITST1 : Test mode input buffer (with pull-down)

2-6. TIMING CONTROL IC (LZ9GG314)

(1) FEATURES

The LZ9GG314 is a timing control IC for TFT-LCD modules.

Applicable model: Modules using QVGA pixel digital driver

(1) Generates, by inputting the clock signal, horizontal synchronous signal, and vertical synchronous signal, the following signals which synchronize with them:

1) Source driver drive signals: CLK, SPL, SPR, LP, PS

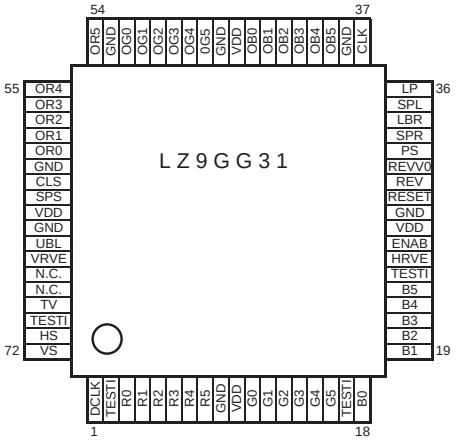
2) Gate driver drive signals: CLS, SPS

3) Signal for generating common electrode drive signal: REV

4) Base signal generation signal: REVV0

(2) Capable of inverting the display screen upside down and horizontally.

(2) PIN CONFIGURATION DIAGRAM

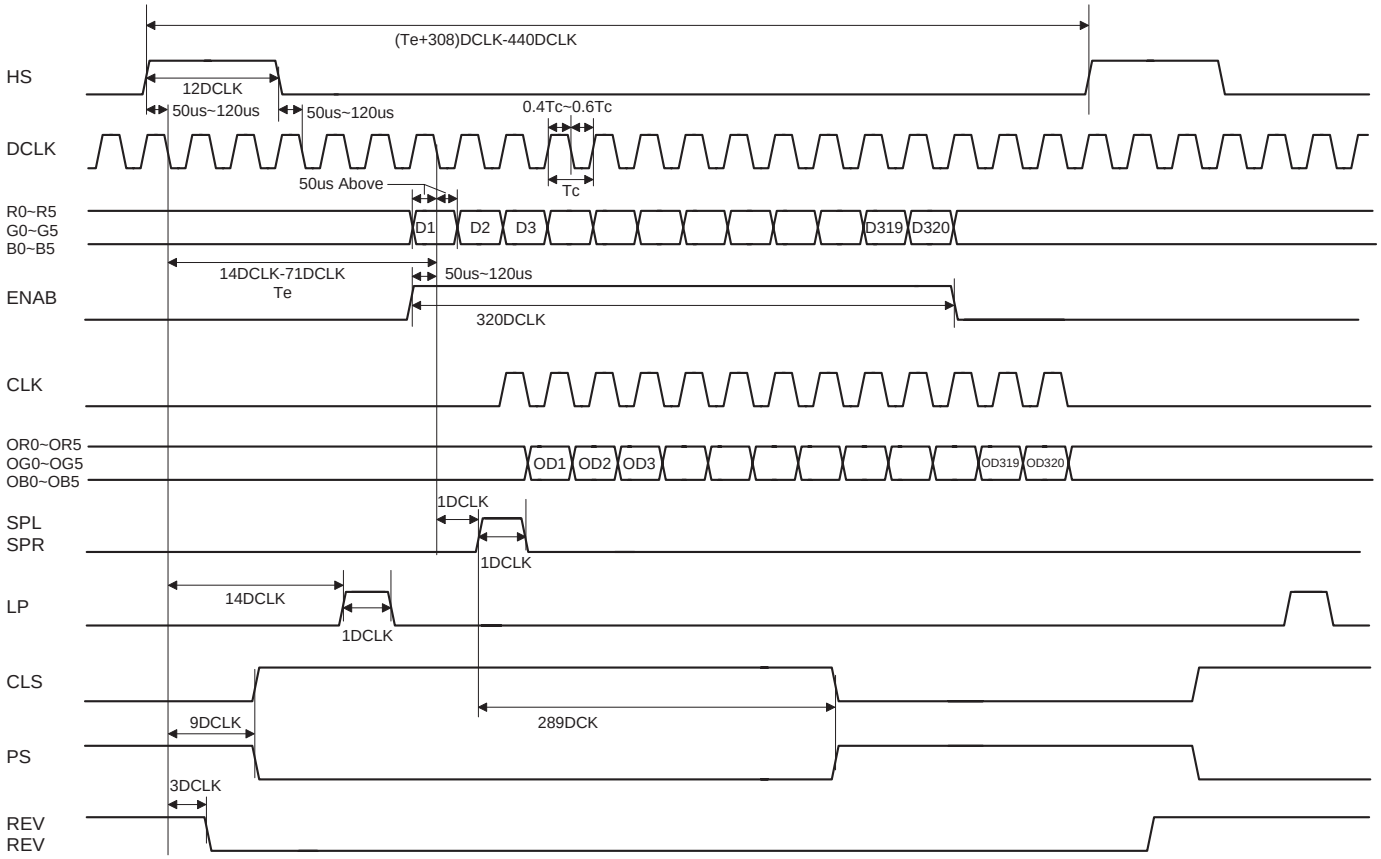

54
37
OR5 GND OG0 OG1 OG2 OG3 OG4 0G5 GND VDD OB0 OB1 OB2 OB3 OB4 OB5 GND CLK
55
OR4 OR3 OR2 OR1 OR0 GND CLS SPS VDD GND UBL VRVE N.C. N.C. TV TESTI HS VS
72
LP SPL LBR SPR PS REVV0 REV RESET GND VDD ENAB HRVE TESTI B5 B4 B3 B2 B1
36
19
LZ9GG31
DCLK TESTI R0 R1 R2 R3 R4 R5 GND VDD G0 G1 G2 G3 G4 G5 TESTI B0
1
18

(3) SIGNAL DESCRIPTION

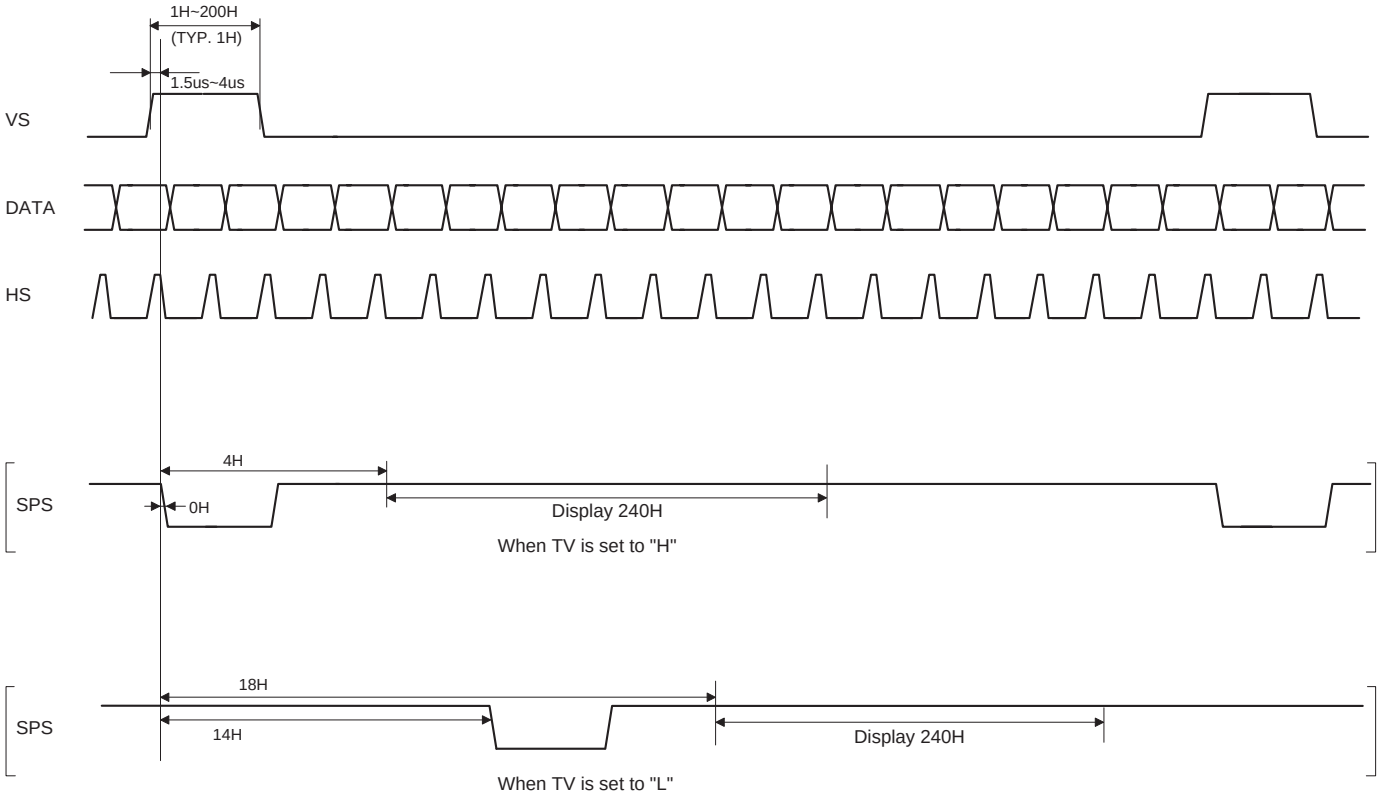
Pin No.	Signal name	Description	I/O
1	DCLK	Data clock signal input pin	I
2	TESTI	Test input pin. Usually set to H	I
3	R0	Red data signal input pin	I
4	R1	Red data signal input pin	I
5	R2	Red data signal input pin	I
6	R3	Red data signal input pin	I
7	R4	Red data signal input pin	I
8	R5	Red data signal input pin (MSB)	–
9	GND	Grounding power supply pin	–
10	VDD	Power supply input pin	I
11	G0	Green data signal input pin	I
12	G1	Green data signal input pin	I
13	G2	Green data signal input pin	I
14	G3	Green data signal input pin	I
15	G4	Green data signal input pin	I
16	G5	Green data signal input pin (MSB)	I
17	TESTI	Test input pin. Usually set to H	I
18	B0	Blue data signal input pin (LSB)	I
19	B1	Blue data signal input pin	I
20	B2	Blue data signal input pin	I
21	B3	Blue data signal input pin	I
22	B4	Blue data signal input pin	I
23	B5	Blue data signal input pin (MSB)	I
24	TESTI	Test input pin. Usually set to H	I
25	HRVE	Right and left inversion setting pin. Usually set to H. Set to L for inversion.	I
26	ENAB	Horizontal display position signal input pin	I
27	VDD	Power supply input pin	–
28	GND	Grounding power supply pin	–
29	RESET	Initialization reset signal input pin. Give the signal which changes L level to H level and holds it when power is turned on	I
30	REV	Common electrode generation signal output pin	O
31	REVV0	Base voltage generation signal output pin	O
32	PS	Source driver control signal output pin	O
33	SPR	Source driver start signal output pin. (High impedance other than when it is used for right and left inversion and ordinary display.)	O
34	LBR	Right and left inversion display control signal output pin HRVE When set to H: H level output When set to L: L level output	O
35	SPL	Source driver start signal output pin (High impedance other than when it is used for right and left inversion and ordinary display.)	O
36	LP	Source driver data transfer signal output pin	O
37	CLK	Source driver clock signal output pin	O
38	GND	Grounding power supply pin	–
39	OB5	Source driver blue data signal output pin (MSB)	O
40	OB4	Source driver blue data signal output pin	O
41	OB3	Source driver blue data signal output pin	O
42	OB2	Source driver blue data signal output pin	O
43	OB1	Source driver blue data signal output pin	O
44	OB0	Source driver blue data signal output pin (LSB)	O
45	VDD	Power supply input pin	–
46	GND	Grounding power supply pin	–
47	OG5	Source driver green signal output pin (MSB)	O
48	OG4	Source driver green signal output pin	O
49	OG3	Source driver green signal output pin	O
50	OG2	Source driver green signal output pin	O
51	OG1	Source driver green signal output pin	O
52	OG0	Source driver green signal output pin (LSB)	O
53	GND	Grounding power supply pin	–
54	OR5	Source driver red data signal output pin (MSB)	O
55	OR4	Source driver red data signal output pin	O
56	OR3	Source driver red data signal output pin	O
57	OR2	Source driver red data signal output pin	O
58	OR1	Source driver red data signal output pin	O
59	OR0	Source driver red data signal output pin (LSB)	O
60	GND	Grounding power supply pin	–
61	CLS	Gate driver clock signal output pin	O
62	SPS	Gate driver start signal output pin	O
63	VDD	Power supply input pin	–

Pin No.	Signal name	Description	I/O
64	GND	Grounding power supply pin	–
65	UBL	Up and down inversion display signal output pin VRVE When set to H: H level output When set to L: L level output	O
66	VRVE	Up and down inversion setting pin. Usually set to H. Set to L for inversion	I
67	N.C.	Non-connection pin. Release electrically.	–
68	N.C.	Non connection pin. Release electrically.	–
69	TV	SPS output timing setting pin	I
70	TESTI	Test input pin. Usually set to H.	I
71	HS	Horizontal synchronous signal input pin (Positive polarity input)	I
72	VS	Vertical synchronous signal input pin (Positive polarity input)	–

Horizontal timing I-b (When ENAB signal is used.)

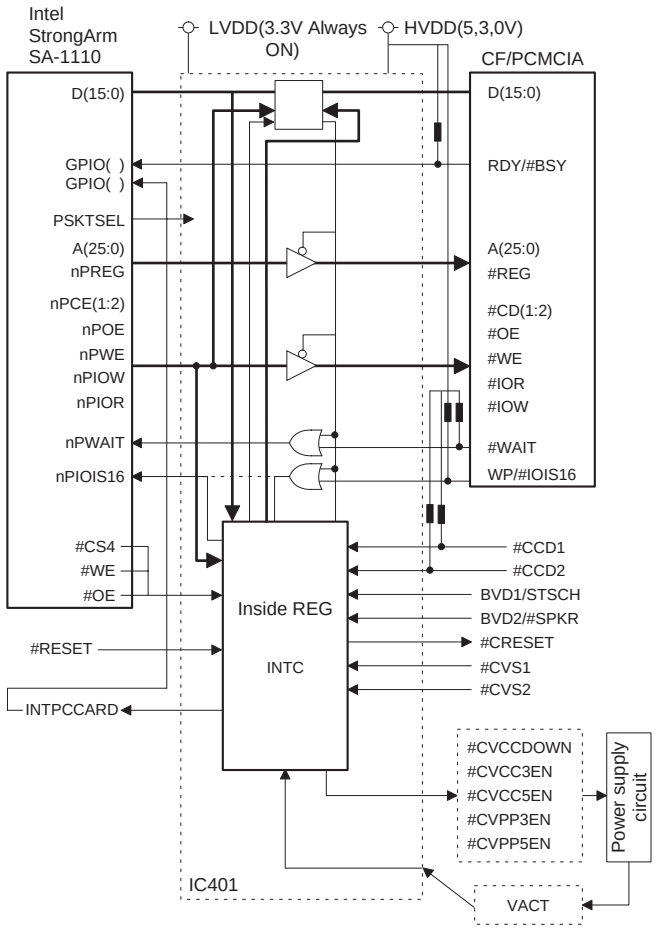


Vertical timing

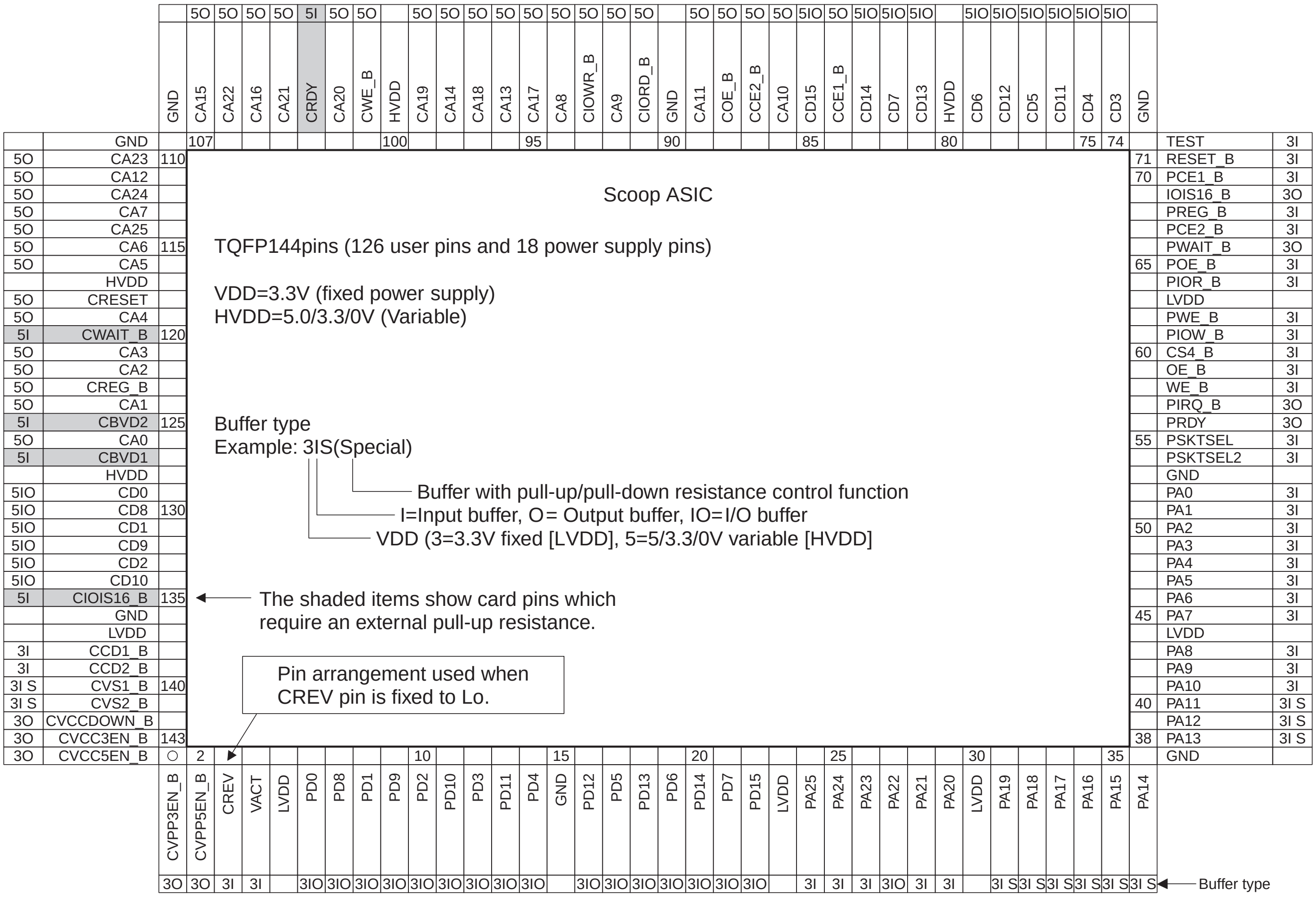


2-7. SCOOP ASIC (S1L50752F26B000)

(1) ASIC CONNECTION OUTLINE



(2) PIN LAYOUT



(3) COMPACT FLASH MODE (GENERAL-PURPOSE I/O TERMINAL)

Since the dedicated Compact Flash mode does not need address lines PA11 - PA22 and CA11 - CA25, they can be used for other purposes. However, it is difficult to use CA11 - CA25 because the card power supply might be turned off. PA11 -PA22 can easily used because LVDD is fixed to 3.3V.

(3)-1. GPIO PINS (PA11 - PA19)

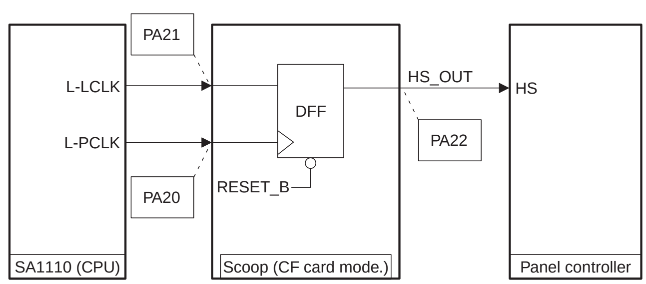
For this reason, pins PA11 to PA19 can be used as general-purpose I/Os according to the setting in the CF mode.

Note:
1. In the CF mode, the above address bus pins are automatically pulled down if set to the GPIO input mode (initial value). The pull-down resistance value is 40k-240kΩ (TYP100kΩ)
2. These pins are basically used for address bus input, and thus input is not Schmitt received.

(3)-2. GLUE-LOGIC PINS [PA20, PA21: INPUT, PA22: OUTPUT]

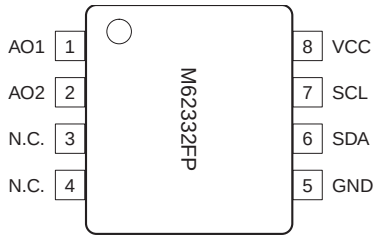
The following logic (DFFx1) is connected to solve the problem with the signal phase relationship between the panel controller and CPU (SA1110).

Circuit diagram

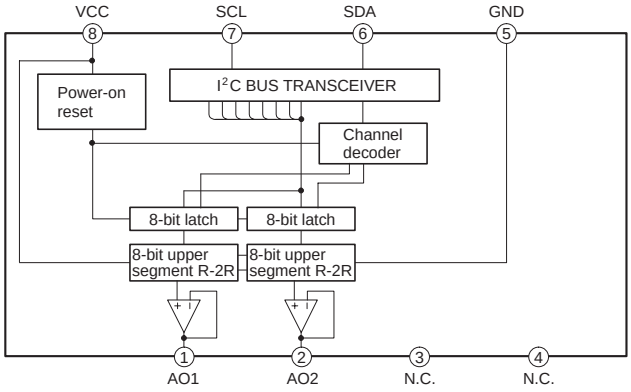


2-8. DAC (M62332)

(1) PIN CONNECTION DIAGRAM



(2) BLOCK DIAGRAM

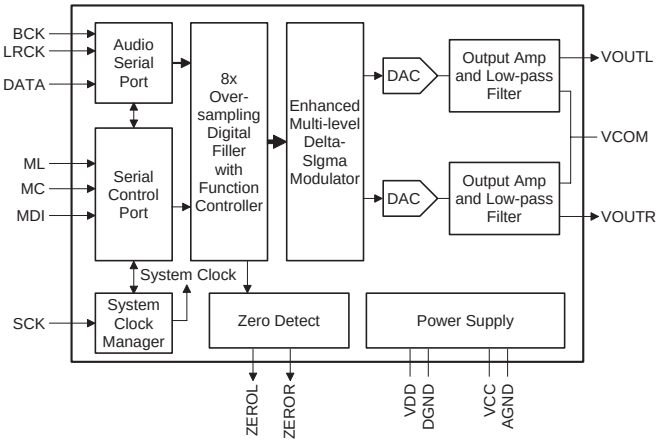


(3) PIN DESCRIPTION

Pin No.	Symbol	Functional description
⑥	SDA	Serial data input pin
⑦	SCL	Serial clock signal input pin
①	AO1	8-bit resolution D/A converter output pin (After power is turned on, all channels are reset and DAC data 00h is outputted.)
②	AO2	
⑧	VCC	Power supply voltage pin
⑤	GND	GND pin

2-9. DAC (PCM1741)

(1) BLOCK DIAGRAM



(2) PIN CONFIGURATION

PCM1741

(3) PIN ASSIGNMENTS

PIN	NAME	TYPE	DESCRIPTIONS
1	BCK	IN	Audio data bit clock input. *1
2	DATA	IN	Audio data digital input. *1
3	LRCK	IN	L-channel and R-channel Audio data latch enable input.
4	DGND		Digital ground.
5	VDD		Digital power supply, +3.3V.
6	VCC		Analog power supply, +3.3V
7	VOUTL	OUT	Analog output for L-channel.
8	VOUTR	OUT	Analog output for R-channel.
9	AGND		Analog ground.
10	VCOM		Common voltage decoupling.
11	ZEROR/ZEROA	OUT	Zero flag output for R-channel/ Zero flag output for L/R-channel.
12	ZEROL/NA	OUT	Zero flag output for L-channel/No assign.
13	MD	IN	Mode control data Input. *2
14	MC	IN	Mode control clock input. *2
15	ML	IN	Mode control latch input. *2
16	SCK	IN	System clock input.

Note: *1 Schmitt trigger input, 5V tolerant.

*2 Schmitt trigger input with internal pull-down, 5V tolerant.

2-10. DC/DC CONVERTER (TEA1206T)

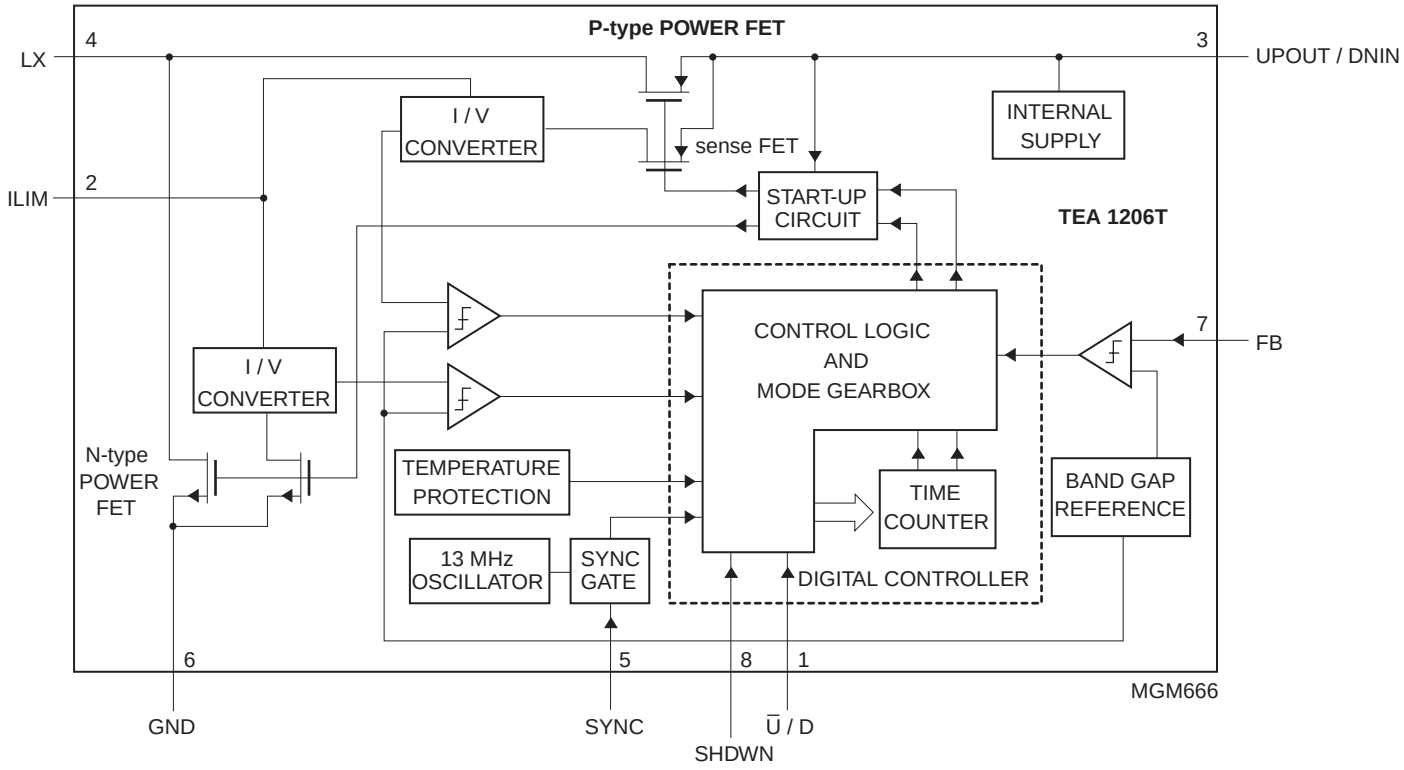
(1) GENELAL DESCRIPTION

The TEA1206T is a fully integrated DC/DC converter. Efficient, compact and dynamic power conversion is achieved using a novel, digitally controlled concept like Pulse Width Modulation (PWM) or Pulse Frequency Modulation (PFM), integrated low RDSon CMOS power switches with low parasitic capacitances, and fully synchronous rectification.

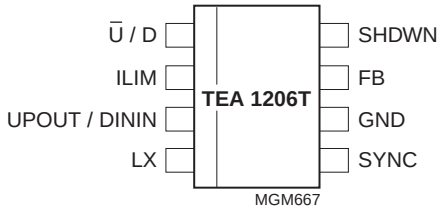
The device operates at 560 kHz switching frequency which enables the use of external components with minimum size. Deadlock is prevented by an on-chip undervoltage lockout circuit.

Efficient behaviour during short load peaks and compatibility with Li-ion batteries is guaranteed by an accurate current limiting function.

(2) BLOCK DIAGRAM



(3) PIN CONFIGURATION

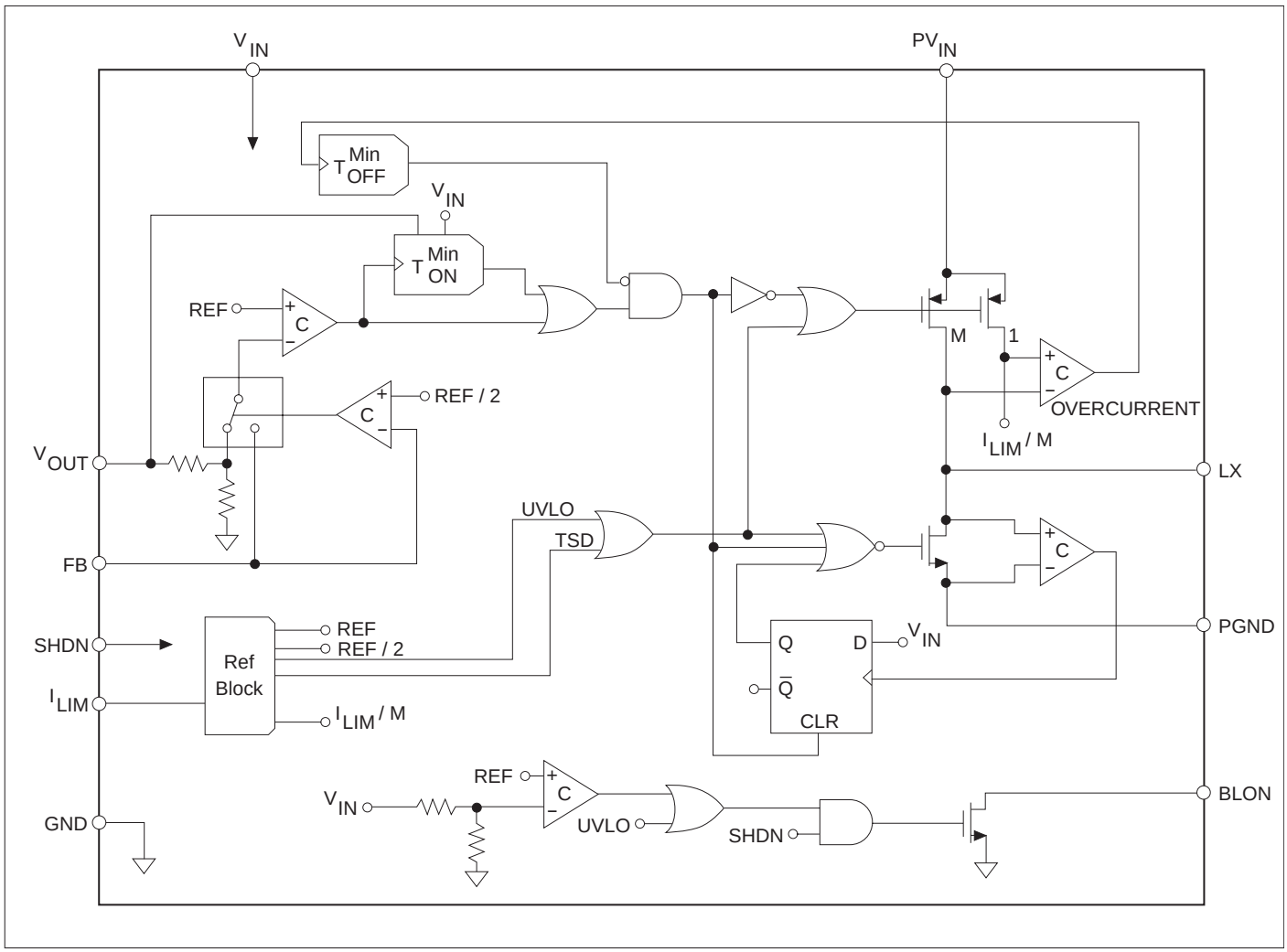


(4) PINNING

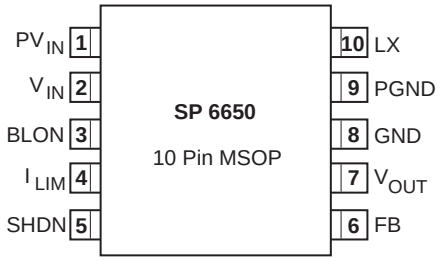
SYMBOL	PIN	DESCRIPTION
$\overline{U}$/D	1	conversion mode selection input
ILIM	2	current limit resistor connection
UPOUT/DNIN	3	upconversion output voltage downconversion input voltage
LX	4	inductor connection
SYNC	5	synchronization clock input
GND	6	ground
FB	7	feedback input
SHDWN	8	shut-down input

2-11. SYNCHRONUS BUCK REGULATOR (SP6650)

(1) BLOCK DIAGRAM



(2) PIN CONFIGURATION



(3) PIN DESCRIPTION

PIN No.	PIN NAME	DESCRIPTION
1	PVIN	Input voltage power pin. Inductor charging current passes through this pin.
2	VIN	Internal supply voltage. Control circuitry powered from this pin.
3	BLON	Open drain battery low output. VIN below battery low threshold pulls this node to ground. VIN above threshold, this node is open.
4	ILIM	Inductor current limit programming pin. Tie pin to VIN for 0.95A peak inductor current limit. Tie pin to ground for 0.5A peak inductor current limit. TTL input threshold.
5	SHDN	Shutdown control input. Tie to VIN for normal operation, tie to ground for shutdown. TTL input threshold.
6	FB	External feedback network input connection. Connect a resistor from FB to ground and FB to VOUT to control the output voltage externally. This pin regulates to the internal bandgap reference voltage of 1.25V. Tie FB to ground to use the internal divider for a preset output voltage of 3.3V.
7	VOUT	Output voltage sense pin. Used for internal feedback divider and timing circuit.
8	GND	Internal ground pin. Control circuitry returns current to this pin.
9	PGND	Power ground pin. Synchronous rectifier current returns through this pin.
10	LX	Inductor switching node. Inductor tied between this pin and the output capacitor to create regulated output voltage.

2-12. HOW TO USE EACH LSI PIN ON THE SL-5500

				SL-5500				
			Direction		I/O			Level at OFF
SA1110	GPIO0	Reserve		ON_KEY	I	from KEY	Default: Both edges enable	
	1	Reserve		AC_IN	I	AC at “H”	Default: Both edges enable	
	2	LCD_8	out	LCD_8	O			LOW
	3	LCD_9		LCD_9	O			LOW
	4	LCD_10		LCD_10	O			LOW
	5	LCD_11		LCD_11	O			LOW
	6	LCD_12		LCD_12	O			LOW
	7	LCD_13		LCD_13	O			LOW
	8	LCD_14		LCD_14	O			LOW
	9	LCD_15		LCD_15	O			LOW
	10	SSP_TXD	out	SDOUT (SSP TI mode)	O			LOW
	11	SSP_RXD	in	Interupt for SD I/O card	I	PullUp	SD I/O CARDinterupt act=”L”	
	12	SSP_SCLK	out	SCLK (SSP TI mode)	O			LOW
	13	SSP_SFRM	out	SFRM (SSP TI mode)	O			LOW
	14	UART_TXD	out	CF_IRQ	I	from_CF_GA	Compatible for both edges	
	15	UART_RXD	in	nREMOCON_INT	I			
	16	GPCLK_OUT	out	TC35143_RESET	O			LOW
	17	Reserve		/MIC_ON	O		Microphone input enable at “L”	LOW
	18	UART_SCLK1	in	nREMOCON_1k_ON	O		Enable at LOW	HI
	19	SSP_CLK	in	STEREO_64FS_CLK	I			
	20	UART_SCLK3	in	CO	I		Charging at LOW (of the charging indicator)	
	21	MCP_CLK	in	9.21MHz	I	from GA	TC35143: Synchroniza-tion clock (SIBCLK)	
	22	TREQA/MBREQ	in	CF_DETECT	I	from_CF_GA		
	23	TREQB	in	TC35143_IRQ	I	from TC35143AF		
	24	Reserve		WAKEUP (16pin)	I	from 16pin conn.		
	25	RTC_CLOCK	out	GA_INT	I	from GA		
	26	RCLK_OUT	out	Main_Batt._LOW	I	Detected externally		
	27	32kHz_OUT	out	32kHz_OUT	O			LOW
	Serial ch0	(USB)		UDC- (USB Function)	I/O			
				UDC+ (USB Function)	I/O			
	Serial ch1	(GPCLK/UART)		TXD1	O		TS only	LOW
				RXD1	I		TS only	INPUT
	Serial ch2	(Infrared)		TXD2	O			LOW
				RXD2	I			INPUT
	Serial ch3	(UART)		UART RXD (16pin connecter)	I			ONPUT
				UART TXD (16pin connecter)	O			LOW
	Serial ch4	(MCP/SSP)		MCP mode (TC35143AF DIN)	O			LOW
				MCP mode (TC35143AF DOUT)	I			INPUT
				NC	O		Use CLK that is inputted from GP21.	LOW
				MCP mode (TC35143AF SIBSYNC)	O			LOW

				SL-5500				
			Direction		I/O			Level at OFF
	L DD7:0				O			LOW
	L FCLK				O			LOW
	L LCLK				O			LOW
	L PCLK				O			LOW
	L bias				O			LOW
UCB TC35143	ADC_0			BATT_TEMP	I			
	ADC_1			Main battery voltage and Backup Batt	I			
	ADC_2			Pushing pressure (Tablet)	I			
	ADC_3			Remote control key	I			
							The power of TC35143AF is turned off.	
	IO_0			Board version	I		SL5000 = “L”/ SL5500 = “H”	The power is turned off.
	IO_1			TABLET_CHECK	O		Pushing pressure check enabled at HI	The power is turned off.
	IO_2			F/L duty input	I		Advisable to make tablet conversion during “L”	The power is turned off.
	IO_3			IR_ON	O		ON at LOW	The power is turned off.
	IO_4			AMP_ON	O		ON at HI	The power is turned off.
	IO_5			Board version	I		SL5000 = “L”/ SL5500 = “L”	The power is turned off.
	IO_6			Sounder bias	O		ON at HI	The power is turned off.
	IO_7			MAIN_BATT_SW_ON	O		ON at HI	The power is turned off.
	IO_8			B/U_BATT_SW_ON	O		ON at HI	The power is turned off.
	IO_9			TEMP_ON	O		ON at HI	The power is turned off.
LOCOMO	GPIO0			RTS	O			LOW
	1			CTS	I			
	2			DSR	I			
	3			DTR	O			LOW
	4			LCD_VSHA_ON	O		ON at HI	LOW
	5			LCD_VSHD_ON	O		ON at HI	LOW
	6			LCD_VEE_ON	O		ON at HI	LOW
	7			LCD_MOD	O			LOW
	8			DAC_ON	O		ON at HI	LOW
	9			F/L_VR	O		Large current (bright) at HI	LOW
	10			PCM_SDATA	O			LOW
	11			PCM_SCK	O			LOW
	12			PCM_SLOAD	O			LOW
	13			nSD_DETECT	I		Detected at LOW	
	14			SD_WP	I		WP state at HI	
	15			SD_VCC_ON	O		ON at HI	LOW
	ADSTART				O			LOW
	CPS				O			LOW
	TFTRESET				O			LOW
	CLK9M				O			LOW
	DACSCK				O			LOW
	LRCLK				O			LOW
	SCL				O			LOW

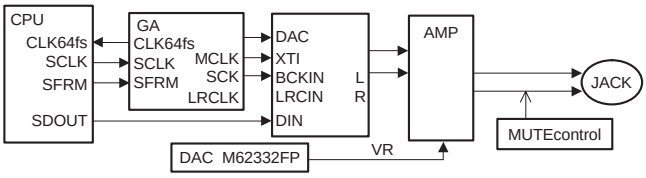
				SL-5500				
			Direction		I/O			Level at OFF
	SDA				I/O			LOW
	CLK64FS				O			LOW
	SPIDO				O		No card / When the set is OFF, con bit falls.	HI-Z
	SPIDI				I		No card / When the set is OFF, con bit falls.	INPUT
	SPICLK				O		No card / When the set is OFF, con bit falls.	HI-Z
	SPICS				O		No card / When the set is OFF, con bit falls.	HI-Z
	SCLK				I			INPUT
	SFRM				I			INPUT
	FLPWM				O			LOW
	MCLK				O			LOW
	18M				CLK			DISABLE
	22M				CLK			DISABLE
	24M				CLK			DISABLE
SCOOP	PA11			CHRG_ON	O		“H” output when charging	Status hold
	PA12			For booting Diag	I		Enabled only when reset start	INPUT
	PA13			For booting Diag	I		Enabled only when reset start	INPUT
	PA14			MUTE_L	O		Earphone mute control: Mute at “L”	LOW
	PA15			MUTR_R	O		Earphone mute control: Mute at “L”	LOW
	PA16			5V_ON	O		Diag ON at “H”/ OFF at “L”	
	PA17			AMP_CN2	O		ON at HI	LOW
	PA18			VPEN_CN2	O		WP cancel at HI (Lock down bit an be changed.)	LOW
	PA19			L/B VOLTAGE CHNG	O		USB D+ signal pull-up resistor control (Enabled at “H”)	LOW
	PA20			LCD TIMING ADJUSTMENT F/F CLK	I			INPUT
	PA21			LCD TIMING ADJUSTMENT F/F DATA	I			INPUT
	PA22			LCD TIMING ADJUSTMENT F/F Q	O			

3. ABOUT THE SYSTEM OF SL-5500

3-1. SYSTEM OUTLINE

Item	SL-5500
CPU	SA1110 Rev.B4
ROMP capacity (x32 bus fixed)	nCS0 → 16MB nCS1 → Not Use nCS2 → Not Use nCS3 → Not Use PC slot A → CF NCS4 → GA/CF_GA NCS5 → Not Use
RAM capacity (SDRAM)	nMCS0 → 64MB nMCS1 → Not Use nMCS → Not Use
Optical communication	IrDA1.2 (115kbps) Sharp:GP2W0110YP
USB (slave only)	USB1.1 (16-pin connector)
Touch panel	Resistance sheet type
LCD	HR-TFT 320 x 240 dots
SD card	Yes
CF card	Type II
F/L brightness control function	Front CCFL Duty light control/VR (current) light control
AUDIO	Sounder & earphone jack DAC:PCM1741 AMP:NJM2172
Analog	TC35143AF
16-pin connector	Charger power supply USB (Function) Serial & JTAG (switchable)

3-2. AUDIO CONTROL



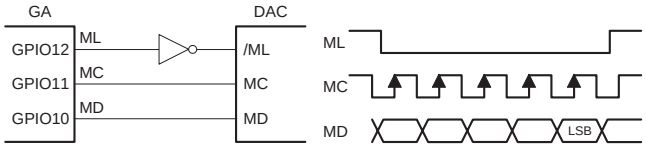
At this time, the clock signal inputted into GPIO19 is used as the synchronous clock signal.

DAC is controlled using GPIO of GA.

/ML :PCM_SLOAD (GPIO12)

MC :PCM_SCK (GPIO11)

MD :PCM_SDATA (GPIO10)



3-3. SERIAL CONTROL

The 16-pin connector has two modes: serial and JTAG. The two modes can be switched over using the pin 13.

Pin assignment of 16 pins

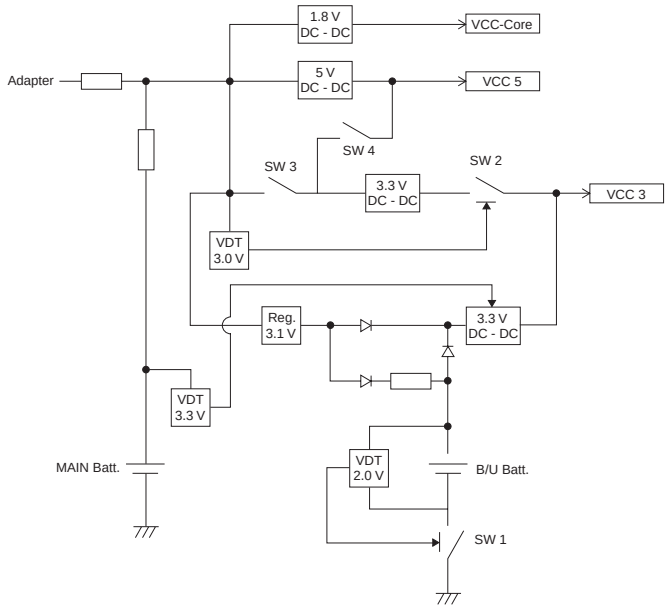
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
13pin L	PWR	PWR	TXD	RXD	RTS	CTS	DSR	GND	USB D+	WU	VCC 3.3V	USB D–	TRST	DTR	PWR	PWR

- When the pin 13 is at LOW, the connector operates in the serial mode.
- Wakeup from 16-pin serial

  Wakeup can be performed using the signal from the pin 10 of the 16-pin connector.

  This causes an event at CPU-GP24 when SW at the cradle is pressed. (Active LOW)

4. POWER SUPPLY COMPOSITION



SW1: Off when the backup battery voltage falls below 2V. (Discharging is inhibited. Charging is allowed.)

SW2: Off when VAB falls below 3V.

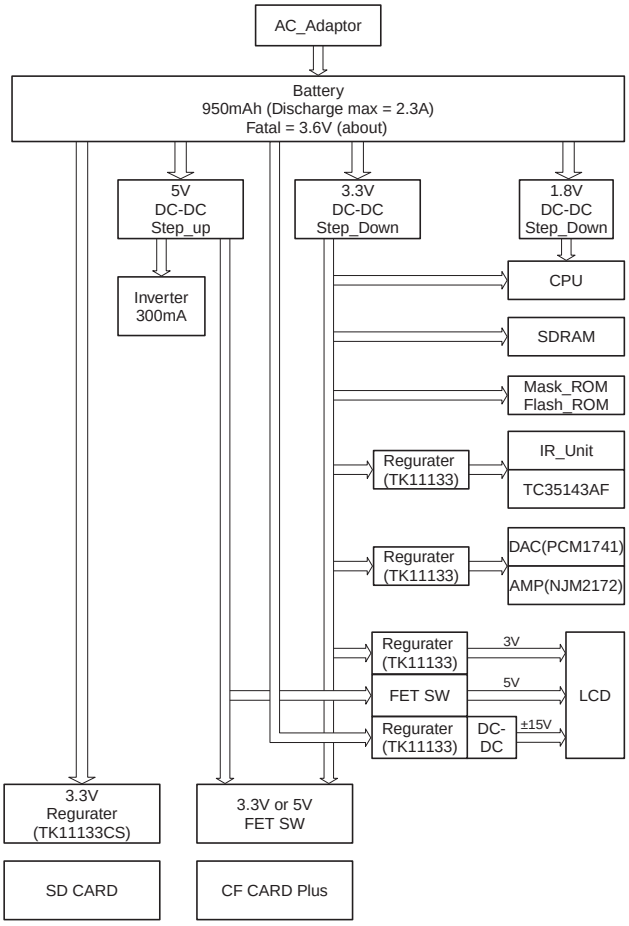
During set ON

5VDC/DC=ON (5V output)
SW3 = ON
SW4 = OFF

During set OFF (Main battery voltage >3.3V)

5V DC/DC=ON (3.8V output)
SW3 = OFF
SW4 = ON

POWER BLOCK DIAGRAM

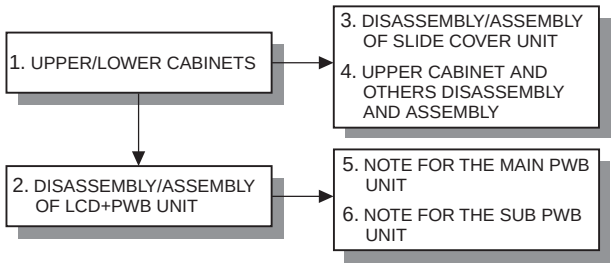


CHAPTER 3. DISASSEMBLY AND ASSEMBLY

This chapter describes the disassembly procedures. For assembly, reverse the disassembly procedures. For points which require special care, descriptions are made in “Note for Assembly.”

For easy and simple replacement procedures of units or parts, descriptions are omitted.

FLOWCHART OF DISASSEMBLY

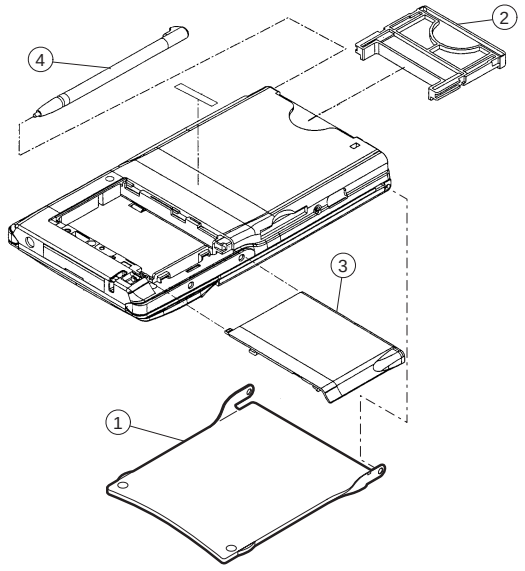

1. UPPER/LOWER CABINETS
2. DISASSEMBLY/ASSEMBLY OF LCD+PWB UNIT
3. DISASSEMBLY/ASSEMBLY OF SLIDE COVER UNIT
4. UPPER CABINET AND OTHERS DISASSEMBLY AND ASSEMBLY
5. NOTE FOR THE MAIN PWB UNIT
6. NOTE FOR THE SUB PWB UNIT

1. UPPER/LOWER CABINETS

1. Remove the Display Protection Cover ①, the CF Slot Protection Card ②, the Battery Compartment Lid ③, the Stylus ④.

PARTS LIST

No.	Parts name
①	Display Protection Cover
②	CF Slot Protection Card
③	Battery Compartment Lid
④	Stylus



∗ Note for assembly

(a) CF Slot Protection Card Installation

① Insert the CF Slot Protection Card into the CF Slot with the note Japanese descriptions facing toward the set. Be sure to confirm the click “Sound” when inserting the card completely.

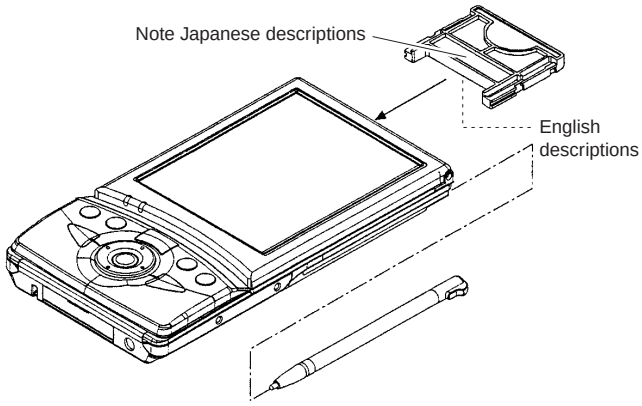
② Remove and insert the card 2 or 3 times to check that insertion is made smoothly.

③ If the card is inserted forcibly in the wrong direction, it may be broken.

(b) Stylus Installation

① Insert the Stylus so that the projection of the Stylus comes in the notch of the set. Be sure to confirm the click “Sound” when inserting the Stylus completely.

② Remove and insert the Stylus 2 or 3 times to check that insertion is made smoothly.



(c) Display Protection Cover Installation

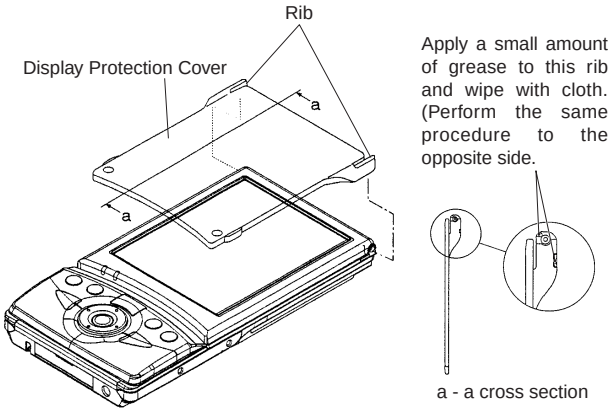
① Apply grease to the Display Protection Cover Rib and wipe with cloth.

② Check that the Display and Upper Cabinet sections around the display are free from scratches, dirt, and dust.

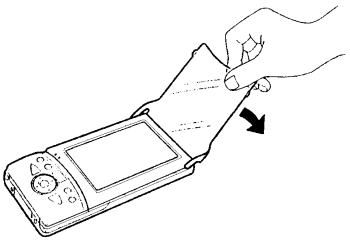
③ Engage the Display Protection Cover Ribs to the set one by one.

④ Be careful not to scratch the Upper Cabinet.

⑤ Check that the Open/Close Lock is switches smoothly.

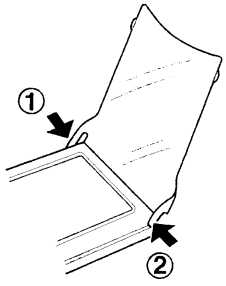

Rib
Display Protection Cover
a
a
Apply a small amount of grease to this rib and wipe with cloth. (Perform the same procedure to the opposite side.
a - a cross section

Disassembly



Pushing the Display Protection Cover more than 135 degrees will cause the cover to come OFF.

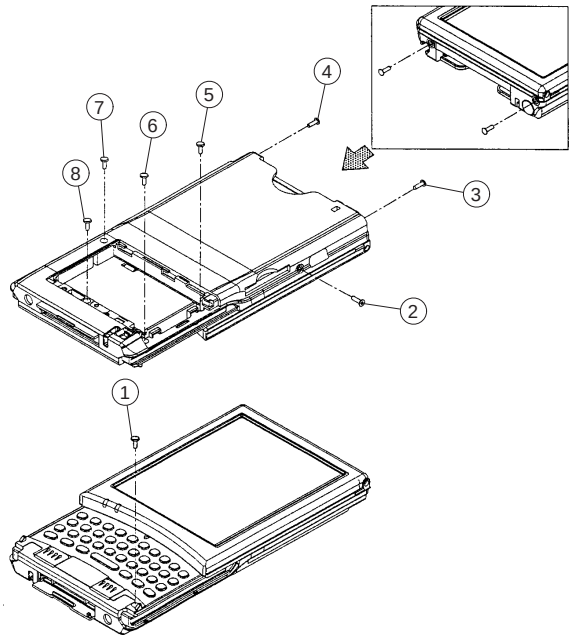
Assembly



When assembling, attach the both sides one by one.

2. For disassembly, remove the Slide Cover Unit and eight screws in the sequence of ①, ② ~ ④, and ⑤ ~ ⑧.

   Note: Do not apply excessive force to the screws and carefully remove them.



∗ Note for assembly

Tighten the screws in the following sequence.

(1) Tighten the screws ⑤ ~ ⑧.

(2) Tighten the screws ② ~ ④.

(3) Tighten the screw ①.

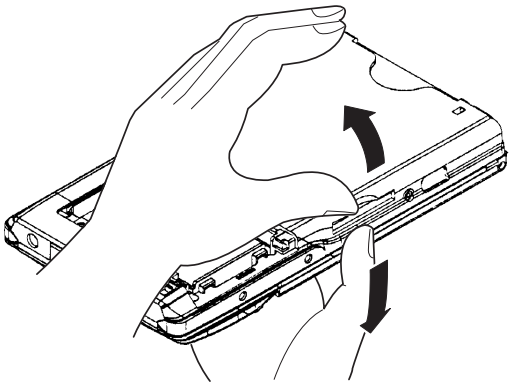
∗ Note for tightening screws

When tightening screws, be careful not to apply an excessive force.

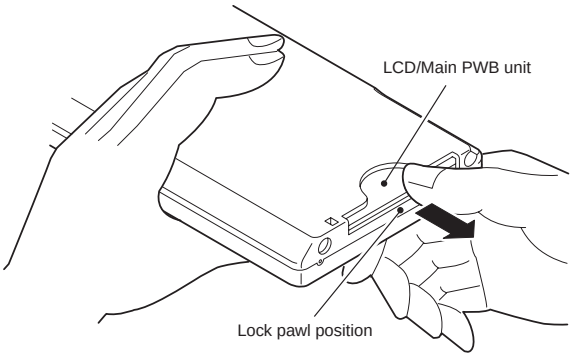
3. Remove the Lower Cabinet.

∗ Lower Cabinet disassembly procedure

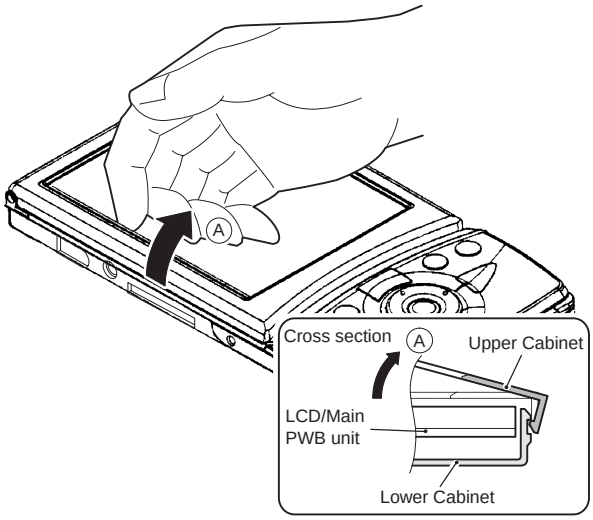
(1) Disengage the upper and the lower cabinets on the right side (SD slot side) when viewed from the back of the SL-5500. Since there is no lock pawl in this section, they can be disengaged with a slight force.



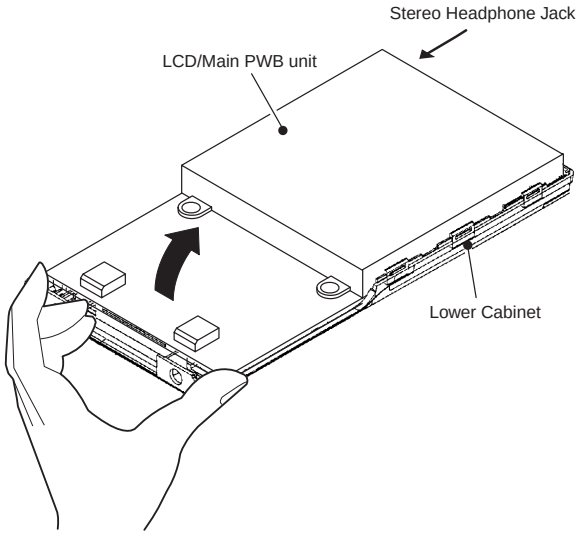
(2) Put your finger in the groove between the LCD/Main PWB unit and the Lower Cabinet, and open and disengage the lock pawl in the arrow direction.



(3) Put your fingers in the clearance between the upper cabinet and the LCD/Main PWB unit, and slowly lift and remove the upper cabinet in the arrow direction Ⓐ.

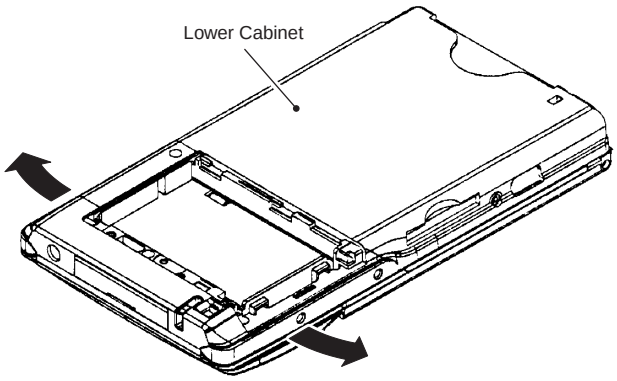


(4) Remove the LCD/Main PWB unit from the Lower Cabinet. In the arrow section, the stereo headphone jack (equipped in the main PWB) is inserted into the hole in the lower cabinet. Be careful not to apply an excessive force to that section, and hold the key side of the LCD/Main PWB unit and slowly lift it upward to remove it from the Lower Cabinet.



Note for removing the Lower Cabinet of the SL-5500

When removing the Lower Cabinet, do not shake the Lower Cabinet right and left. If it should be shaken with an excessive force, the boss on the Lower Cabinet would hit and damage component parts (L601, L602) on the main PWB unit.



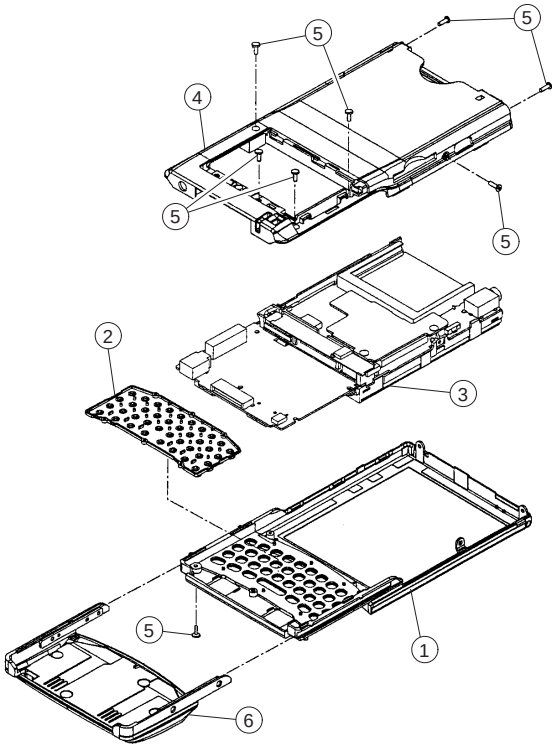
CAUTION

When disassembling the lower cabinet, be sure to check and confirm visually (with a magnifying glass) that the components (L601, L602) are normally soldered on the main PWB unit.

[BASIC COMPOSITION OF ASSEMBLY PARTS]

PARTS LIST

No.	Part name
①	Upper Cabinet Unit
②	Key Rubber A
③	LCD + PWB Unit
④	Lower Cabinet Unit
⑤	Screw C
⑥	Slide Cover Unit



[NOTE FOR ASSEMBLY]

1. Battery Take-Out Ribbon attachment

   (1) Clean and remove oil from with IPA from the ribbon attachment sections (2 positions) of the Lower Cabinet.

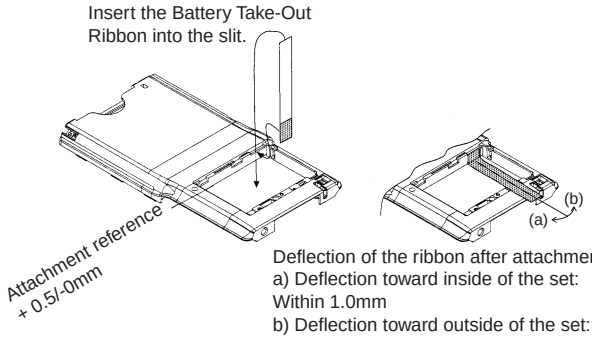
   (2) Attach the Battery Take-Out Ribbon to the inside of the Battery Storage section.

   (3) Pass the Battery Take-Out Ribbon through the slit of the Lower Cabinet and wind it around.

   (4) Fold the Battery Take-Out Ribbon, and attach the Duplex Tape of the other half of the ribbon to the outside of the Battery Storage section.

   (5) Press the attachment section to assure attachment.

   Note: After attachment, remove oil from the attachment section in order to prevent the ribbon from coming off.

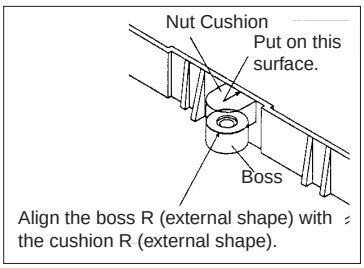


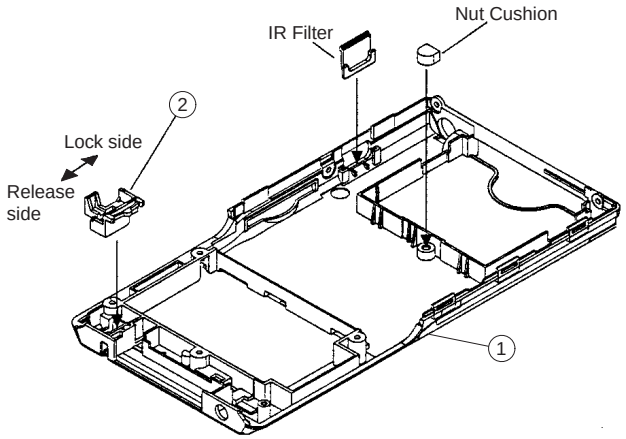
Deflection of the ribbon after attachment
a) Deflection toward inside of the set: Within 1.0mm
b) Deflection toward outside of the set: Not allowed.

2. Assembly of the Battery Replacement Switch and the IR Filter and the Nut Cushion

   (1) Attach the Battery Replacement Switch ② to the Lower Cabinet ①.

   (2) When attaching the Lower Cabinet, be sure to set the Battery Replacement Switch ② to the LOCK position. If not, the Battery Replacement Switch may break.

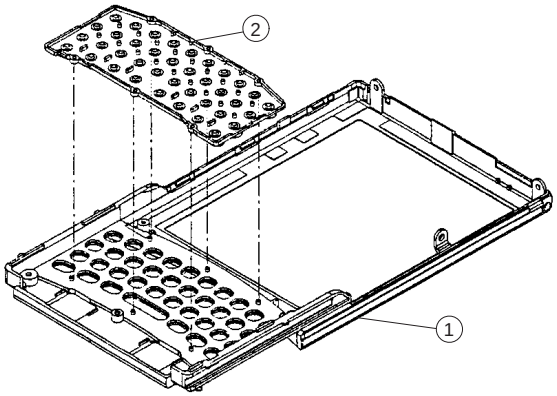




3. Note for assembly of Key Rubber A

   (1) Insert the positioning ribs (x 6) of the Upper Cabinet Unit ① into the positioning holes of the Key Rubber ②.

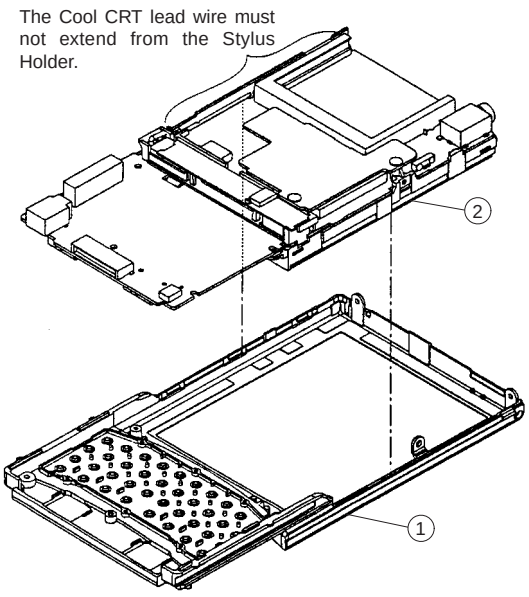
   (2) Attach so that the rubber does not cover the cabinet holes.



4. Note for assembly of the LCD + PWB Unit to the Upper Cabinet Unit

   (1) Attach the LCD + PWB Unit ② to the Upper Cabinet Unit ① from the Stylus Holder side.

   (2) Be careful not to pinch the lead wire (white) of the Cool CRT. If it should be pinched, check that the coating of the lead wire is not damaged. (Never use a lead wire with breakage or damage.)



5. Note for assembly of the Lower Cabinet Unit

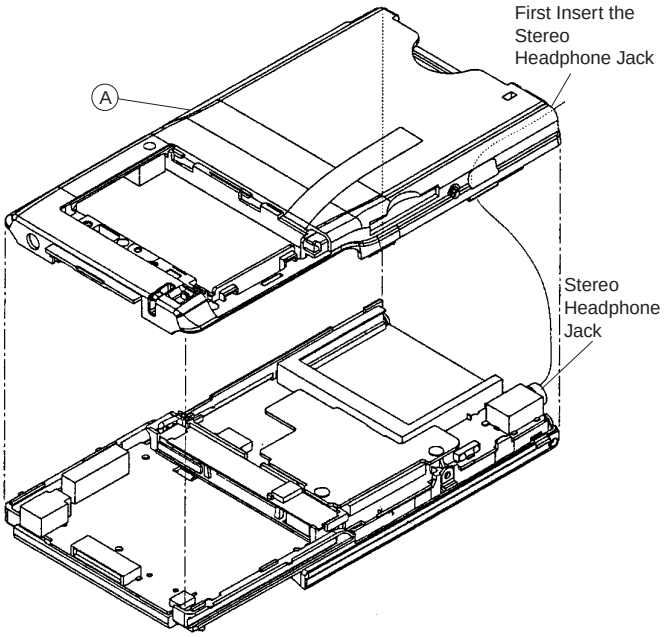
   (1) Check that the following parts are attached to the Lower Cabinet Unit Ⓐ.
   IR Filter, Battery Replacement Switch, I/O Cover, I/O Holder, Battery Take-Out Ribbon, Nut Cushion

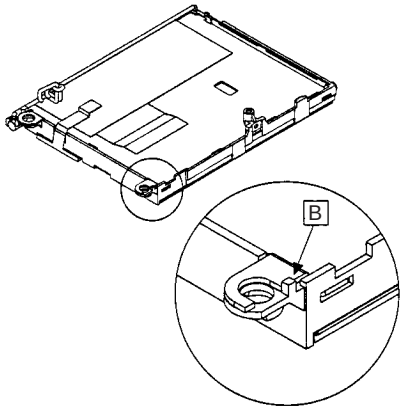
   (2) First, insert the Stereo Headphone Jack of the Lower Cabinet Unit Ⓐ, then engage the Pawls.

   (3) Be careful not to pinch the lead wire (white) of the Cool CRT. If it should be pinched, check that the coating of the lead wire is not damaged. (Never use a lead wire with breakage or damage.)

   (4) If the parts are engaged forcibly, they may be broken.

   (5) Check that there is no bending when engaging.



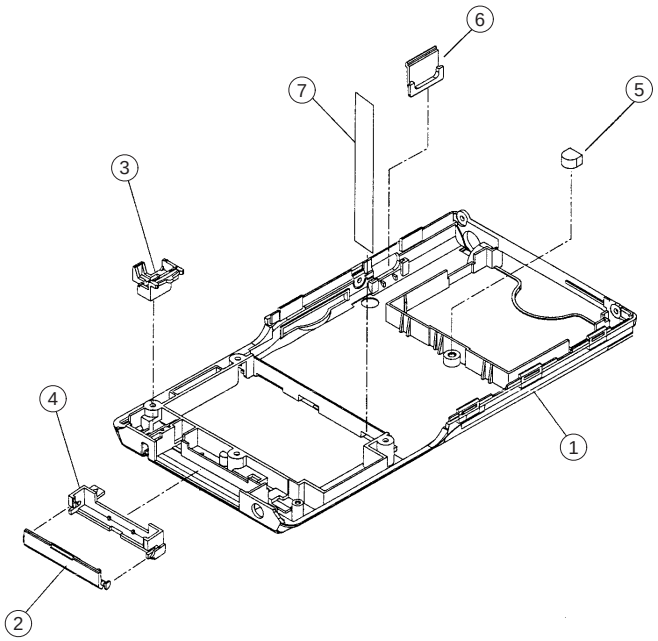


Check that the PWB is not on the LCD holder rib B when assembling the lower cabinet.
(If it is on, an assembly error will occur.)

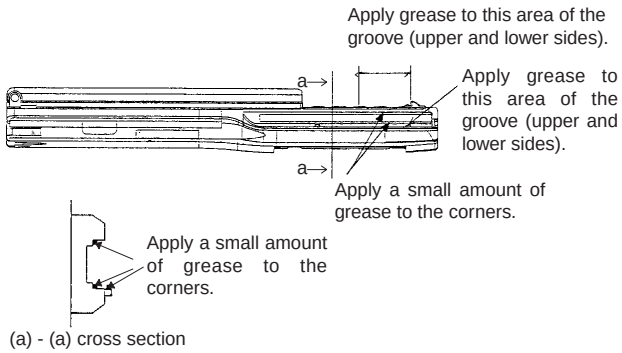
[LOWER CABINET UNIT]

PARTS LIST

No.	Part name
①	Lower Cabinet
②	I/O Cover
③	Battery Replacement Switch
④	I/O Holder
⑤	Nut Cushion
⑥	IR Filter
⑦	Battery Take-Out Ribbon

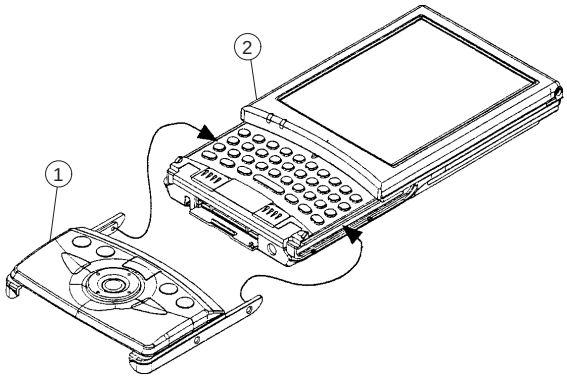


6. Applying Grease to the Slide Cover Slide section
   Apply grease to the upper and lower sides of the sliding section of the Left and Right Upper Cabinets.
   Amount of application: Apply a very small amount of grease to the sides (0.5mm.□)
   Wipe excessive grease with cloth.


Apply grease to this area of the groove (upper and lower sides).
a→
Apply grease to this area of the groove (upper and lower sides).
a→
Apply a small amount of grease to the corners.
Apply a small amount of grease to the corners.

(a) - (a) cross section

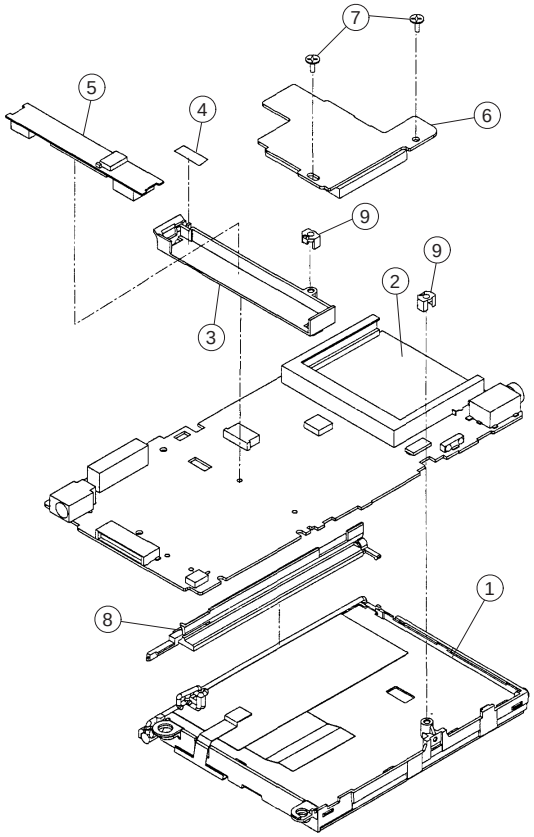
7. Assembly of Slide Cover Unit
   (1) Clean and remove oil with IPA from the Key PWB, the contact pins, and the Key PWB Shielding Sheet on the back of the Slide Cover Unit ①.
   (2) Engage one side of the Slide Cover Fixture of the Slide Cover Unit ① into the sliding groove of the Upper Cabinet ②.
   (3) Extend the arm of the Slide Cover Unit ① and engage the other side of the Slide Cover Fixture into the sliding groove.
   (4) Hold the sides of the Slide Cover Unit ① and slide it back and forth 3 times to apply grease evenly. (Check at the same time that it slides smoothly.)
   (5) Open the Slide Cover Unit ① fully and check that the contact spring is not deformed when viewed from the set sides and the I/O Port.
   (6) When assembling, be careful not to scratch the Upper Cabinet and damage the Upper Cabinet and Fixed Key Panel.
   (7) When assembling, be careful not to deform the contact spring.



2. DISASSEMBLY/ASSEMBLY OF LCD + PWB UNIT

PARTS LIST

No.	Part name
①	LCD Unit
②	Main PWB Unit
③	Inverter Holder
④	Inverter Fixing Tape
⑤	Inverter Unit
⑥	Sub PWB Unit
⑦	Screw D
⑧	Stylus Holder
⑨	Boss Cap



[NOTE FOR DISASSEMBLY/ASSEMBLY OF THE LCD + PWB UNIT]

The disassembly procedures of the LCD + PWB Unit are as follows:

The descriptions are made in the following sequence. Check the notes.

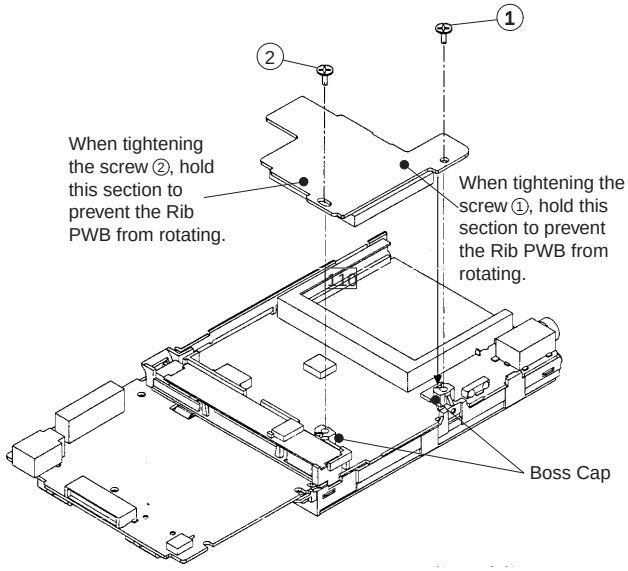
1. Sub PWB Unit disassembly
2. Inverter Unit disassembly
3. Inverter Holder disassembly
4. Stylus Holder disassembly
5. LCD Unit disassembly

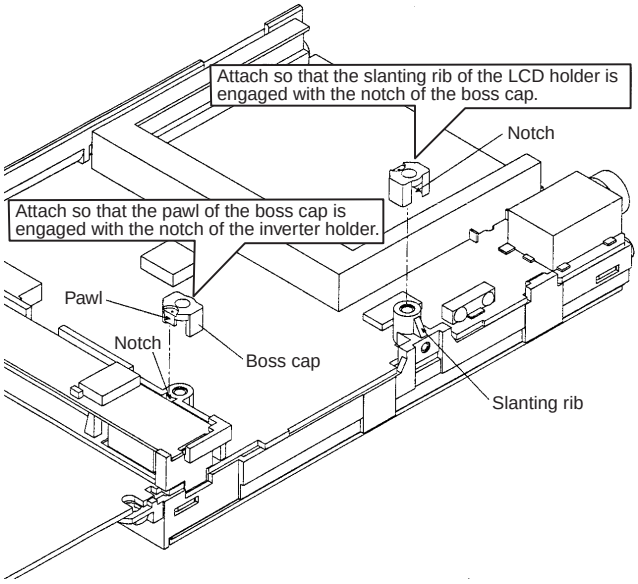
1. Sub PWB Unit disassembly

   Remove screws ① and ②, and remove the Sub PWB Unit.

   ∗ Note for assembly

   - Before assembling the Sub PWB unit, attach two Boss Caps as shown in the figure below.
   - Insert the B-to-B connector straightly. After insertion, do not twist it or do not apply a load to it. (It would cause disconnection of the connector.)
   - Tighten the screws in the sequence of ① to ②.
   - When tightening the screws, do not apply an excessive force.


1
2
When tightening the screw ②, hold this section to prevent the Rib PWB from rotating.
When tightening the screw ①, hold this section to prevent the Rib PWB from rotating.
Boss Cap


Attach so that the slanting rib of the LCD holder is engaged with the notch of the boss cap.
Notch
Attach so that the pawl of the boss cap is engaged with the notch of the inverter holder.
Pawl
Notch
Boss cap
Slanting rib

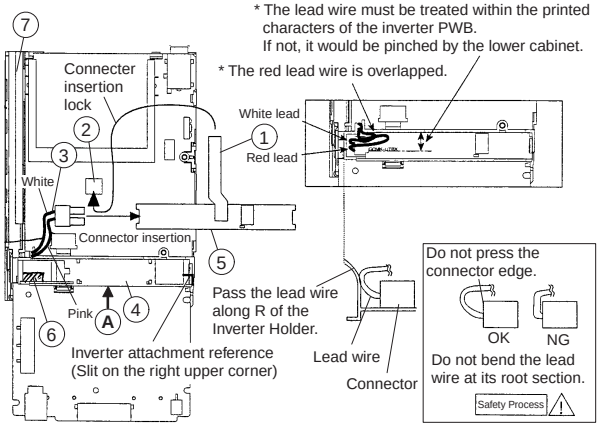
2. Inverter Unit disassembly

Perform the following procedures:

a. Remove the Inverter FPC ① from the Inverter FPC Connector ②.

b. Lift the Inverter Unit from Ⓐ in the figure above, and remove it.

c. Remove the Cool CRT lead connector from the inverter.


* The lead wire must be treated within the printed characters of the inverter PWB. If not, it would be pinched by the lower cabinet.
* The red lead wire is overlapped.
Connecter insertion lock
White lead
Red lead
White
Connector insertion
Pink
Pass the lead wire along R of the Inverter Holder.
Inverter attachment reference (Slit on the right upper corner)
Lead wire
Connector
Do not press the connector edge.
OK
NG
Do not bend the lead wire at its root section.
Safety Process

∗ Note for assembly

(1) Put two lead wires of the Cool CRT ③ in the notch of the Inverter Holder ④.

(2) Connect the lead wire of the Cool CRT ③ to the Inverter Unit ⑤.

(3) Separate the Separation Sheet of the Inverter Fixing Tape ⑥.

(4) First, engage the PWB edge of the Inverter Unit ⑤ on the right upper section of the Inverter Holder ④. Then, put the opposite side of the unit in the holder.

(5) Press and connect the upper section of the connector of the Inverter Unit ⑤.

(6) Release locking of the connector of the Inverter FPC of the Main PWB Unit.

(7) Insert the Inverter FPC completely into the connector and lock it.

(8) Check the connection state.

Reference: Check that the FPC Support Plate can be seen by about 2.0mm from the edge of the connecter lock.

(9) Fold the excessive lead wire of the Cool CRT ② inside the Inverter Holder ④.

(10) Process the lead wire of the Cool CRT ③ so that it does not make contact with the Stylus Lock section of the Stylus Holder ⑦. If not, the Stylus would not be inserted or removed smoothly.

(11) When separating the Separation Sheet of the Inverter Fixing Tape ⑥, be careful to prevent the Duplex Tape from getting entangled.

(Special note)

The Inverter Unit generates a high voltage which may generate heat and smoke if treated improperly.

Therefore, the following notes should be strictly observed.

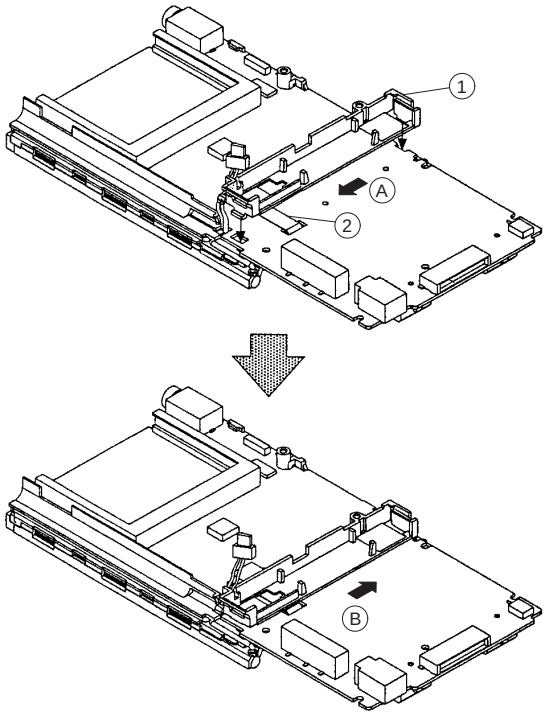
(1) When processing the lead wire of the Cool CRT, be careful not to damage the coating cover.

- Never use a sharp cutter for processing of the lead wire.
- Never use the Cool CRT with damaged or broken coating cover of lead wire.
- Never use an inverter unit that was dropped or damaged by a strong shock.

(2) Since the PWB of the Inverter Unit ⑤ is fragile, be sure to hold the connectors when connecting the lead wire of the Cool CRT ③.

3. Inverter Holder disassembly

Slide the Inverter Holder in the direction of Ⓑ in the figure below, and remove it.



∗ Note for assembly

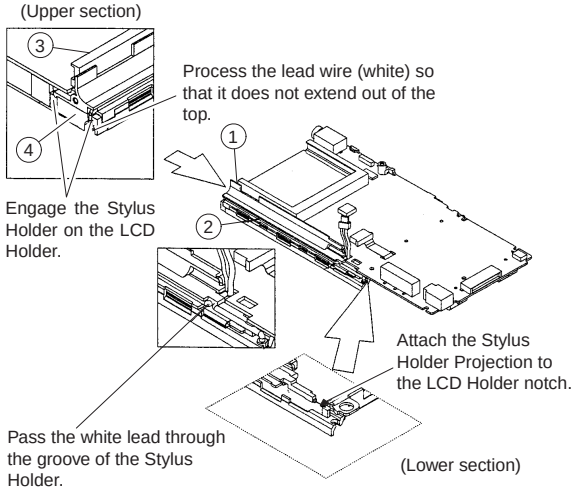
(1) Insert the Pawls (x 2) on the back of the Inverter Holder ① into the hole the notch of the PWB. Then slide the holder to the left in the direction of Ⓐ and fix it.

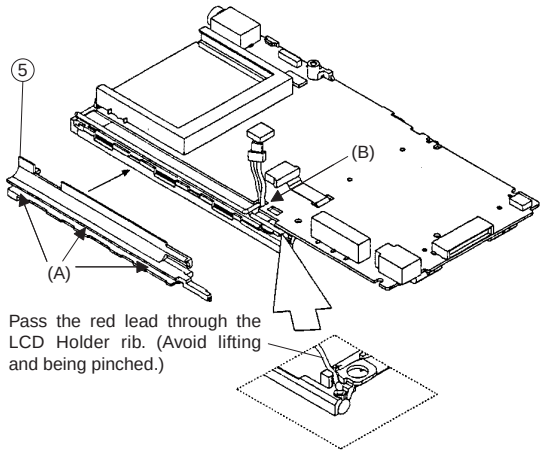
(2) Before attaching the Inverter Holder, check that the Tablet Pin ② is connected.

(3) When attaching, be careful not to damage the lead wire of the Cool CRT.

4. Stylus Holder disassembly

Remove the Cool CRT lead wire (white) ② from the Stylus Holder ①, and remove the holder.


(Upper section)
Process the lead wire (white) so that it does not extend out of the top.
Engage the Stylus Holder on the LCD Holder.
Attach the Stylus Holder Projection to the LCD Holder notch.
Pass the white lead through the groove of the Stylus Holder.
(Lower section)



∗ Note for assembly

(1) Insert the Cool CRT lead wire (white) into the groove (A) of the Stylus Holder ⑤. (Provisional wiring)

(2) Insert the Cool CRT lead wire (red) into the notch of the PWB (B).

(3) Insert the PWB fixing groove of the Stylus Holder into the PWB, and attach the Pawls (one in the lower section, two in the upper section) to the LCD Holder and fix them. (← First attach the Lower Pawl.)

(4) Pull the Cool CRT lead wires (red / white) to the connector side to remove slack.

(5) If there is slack in the lead wire, it cannot be assembled to the Upper Cabinet. Remove slack completely.

(6) When removing slack in the lead wire, do not hold and pull the connector. It may cause breakage of the lead wire.

(Special note)

The Inverter Unit generates a high voltage which may generate heat and smoke if treated improperly.

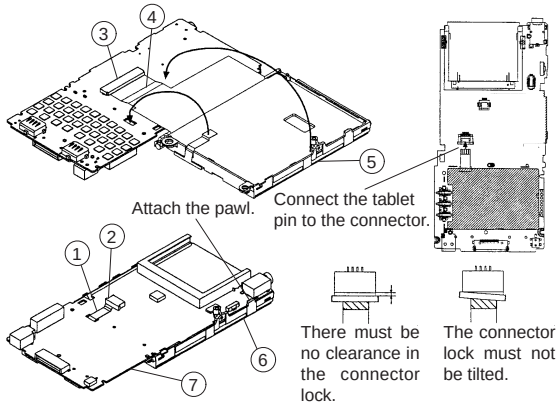
Therefore, the following notes should be strictly observed.

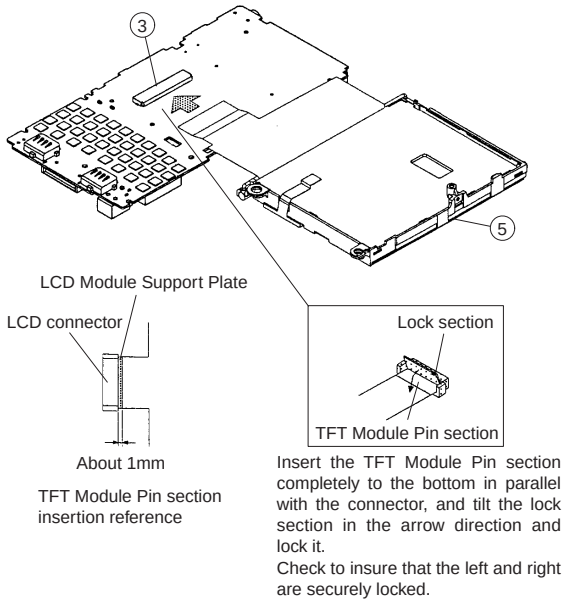
(1) When processing the lead wire of the Cool CRT, be careful not to damage the coating cover.

- Never use a sharp cutter for processing of the lead wire.
- Never use the Cool CRT with damaged or broken coating cover of lead wire.

5. LCD Unit disassembly

Remove the Tablet Pin ① from the connector ②. Remove the PWB from the LCD Unit and reverse it. Remove the LCD Unit FPC ④ from the FPC connector ③.


Attach the pawl.
Connect the tablet pin to the connector.
There must be no clearance in the connector lock.
The connector lock must not be tilted.


LCD Module Support Plate
LCD connector
Lock section
TFT Module Pin section
About 1mm
TFT Module Pin section insertion reference
Insert the TFT Module Pin section completely to the bottom in parallel with the connector, and tilt the lock section in the arrow direction and lock it.
Check to insure that the left and right are securely locked.

∗ Note for assembly

(1) Release locking of the FPC connector ③, and insert the FPC of the LCD Unit ⑤ completely to the bottom in parallel.

(2) Lock the FPC connector ③.

(3) Check the connection state.

Reference: Check that the FPC Support Plate can be seen by 1.0mm from the edge of the connector lock.

(4) When locking, use an anti-static-electricity holder to prevent the PWB from being deflected.

(5) Be careful to prevent breakage of Lock Pawl of the connector.

(6) Bend the FPC of the LCD Unit ⑤ and cover it over the PWB.

(7) Hang the LCD Holder ⑥ Pawl on the PWB Unit ② and fix it.

(8) Pass the Tablet Pin ① through the slit of the PWB.

(9) Release locking of the connector on the opposite side of the PWB, and insert the Tablet Pin ①.

(10) Lock the connecter.

(11) Check the connection state.

Reference: Check that the Tablet Pin pattern (silver color) is hidden by the connecter completely.

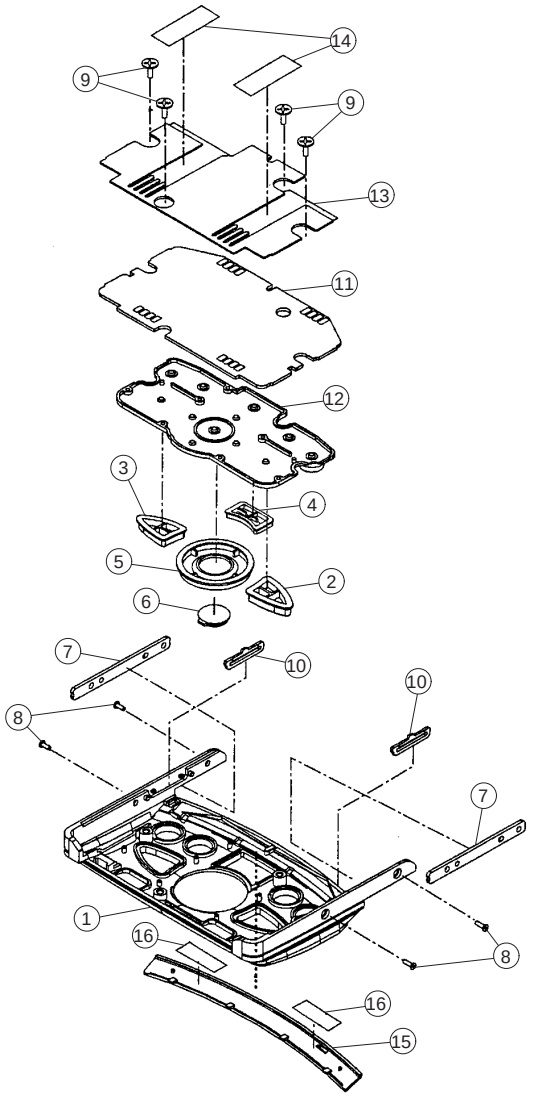
(12) Check that the PWB Unit ⑦ is securely fixed by the LCD Holder ⑥ Pawl.

(13) The tablet pin ① cannot be connected after attaching the Inverter Holder. Be careful to connect securely.

3. DISASSEMBLY / ASSEMBLY OF SLIDE COVER UNIT

PARTS LIST

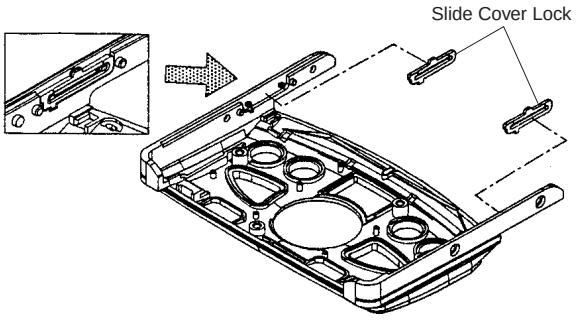
No.	Part name
①	Slide Cover Cabinet
②	Key Top A1 (Cancel)
③	Key Top A2 (OK)
④	Key Top A3 (HOME)
⑤	Key Top B (Cursor)
⑥	Key Top C (Center)
⑦	Slide Cover Fixture
⑧	Screw A
⑨	Screw B
⑩	Slide Cover Lock
⑪	Key PWB Unit
⑫	Key Rubber B
⑬	Key PWB Shielding Sheet
⑭	Sliding Sheet A
⑮	Slide Cover Panel
⑯	Slide Cover Panel Fixing Tape



[NOTE FOR ASSEMBLY OF THE SLIDE COVER UNIT]

1. Slide Cover Lock (x 2) assembly

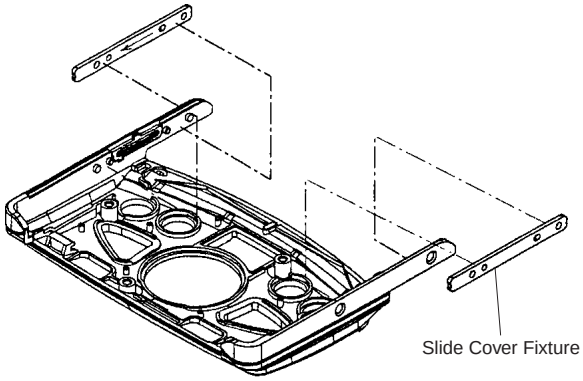
   As shown in the figure below, insert the cover lock into the groove of the cabinet. (Right and left sides)



2. Slide Cover Fixture (x 2) assembly

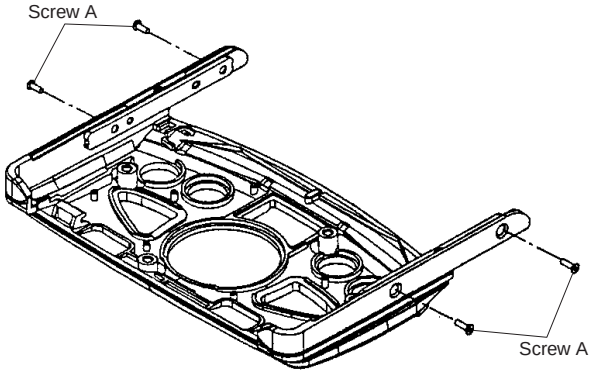
   Attach so that the indication of "↓" on the fixture is as shown in the figure below. (Right and left sides)

   Check that the Slide Cover is fixed to the cabinet rib at two positions.



3. Screw A (x 4) tightening

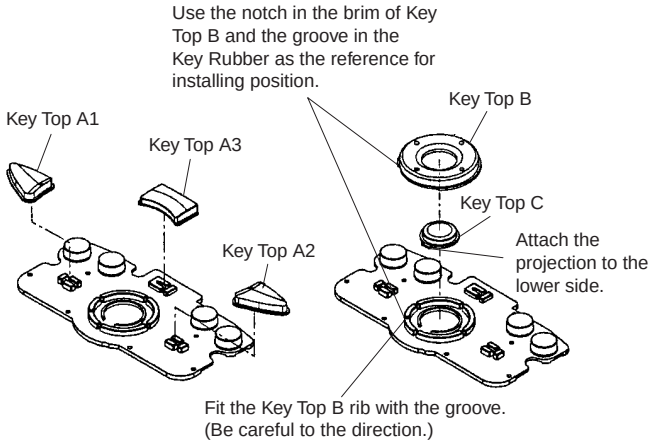
   Be careful not to apply an excessive force.

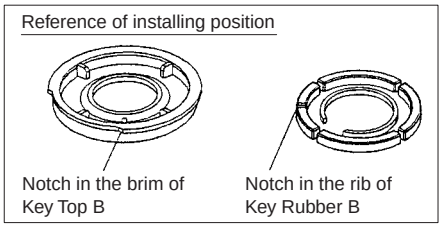


4. Key Top A1, A2, A3, B, C assembly

Engage the Key Rubber B rim with the groove on the back of each key top.

Note: Be careful not to damage the Key Top Projection.


Use the notch in the brim of Key Top B and the groove in the Key Rubber as the reference for installing position.
Key Top A1
Key Top A3
Key Top B
Key Top C
Key Top A2
Attach the projection to the lower side.
Fit the Key Top B rib with the groove. (Be careful to the direction.)



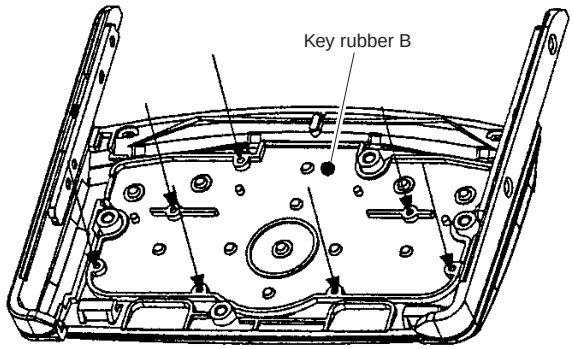
5. Key Rubber B assembly

Push and fit the Key Rubber B positioning holes (↓ 7 positions) with 7 ribs of the Slide Cover Cabinet.

Note: (1) Before installing the Key Rubber B, check that each Key Top is securely installed.

(2) When taking/reversing the Key Rubber B, be careful not to drop the Key Top.

(3) Be careful to prevent the Key Rubber/Key Top from covering the cabinet ribs and key holes.



6. Key PWB Unit assembly

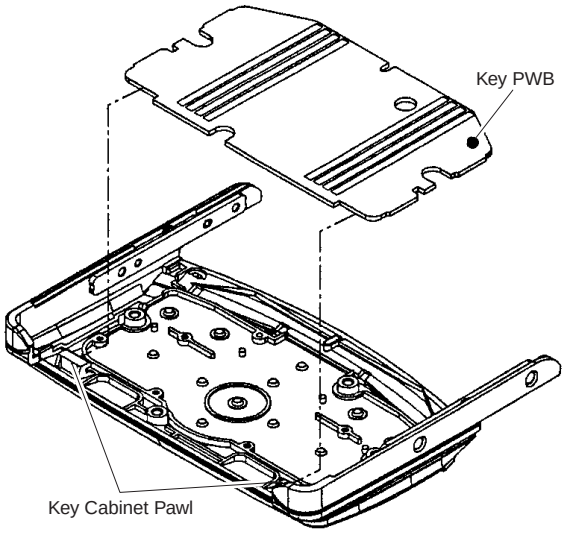
(1) Fit the Slide Cover Cabinet positioning rib with the notch of the Key PWB.

(2) Attach the Key Cabinet Pawls (2 positions) to the Key PWB.

Note: (1) Before installing the Key PWB, check that the Key Rubber and the Key Top do not cover the cabinet rib and the key hole.

(2) Do not touch the pattern section of the PWB to keep the pattern section clean.

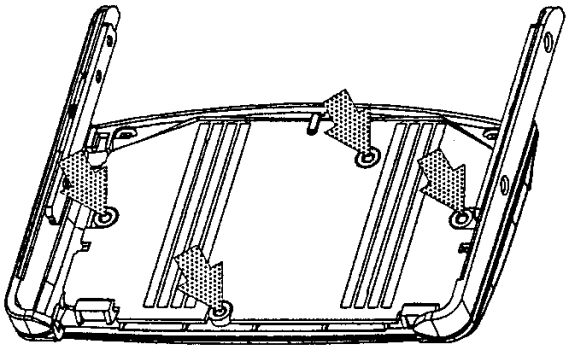
(3) Be careful that the PWB notch and boss holes do not cover the Key Cabinet rib and boss.



7. Screw B (x 4) tightening

(1) Be careful not to apply an excessive force.

(2) Do not touch the PWB contact with bare hands.



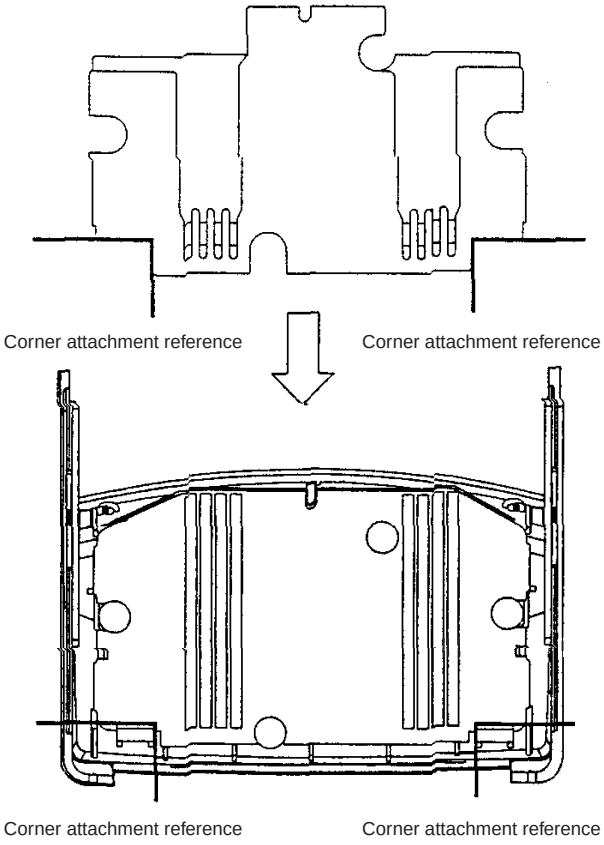
8. Key PWB Shielding Sheet attachment

(1) Clean and remove oil with IPA from the contact pins of the PWB.

(2) Separate the Separation Paper of the Shielding Sheet.

(3) Fit the right and left notches of the Shielding Sheet with the cabinet pawl which are engaged with the PWB.

Note: Be careful that the sheet must not cover the cabinet pawl and screws.



9. Sliding Sheet A (x 2) attachment

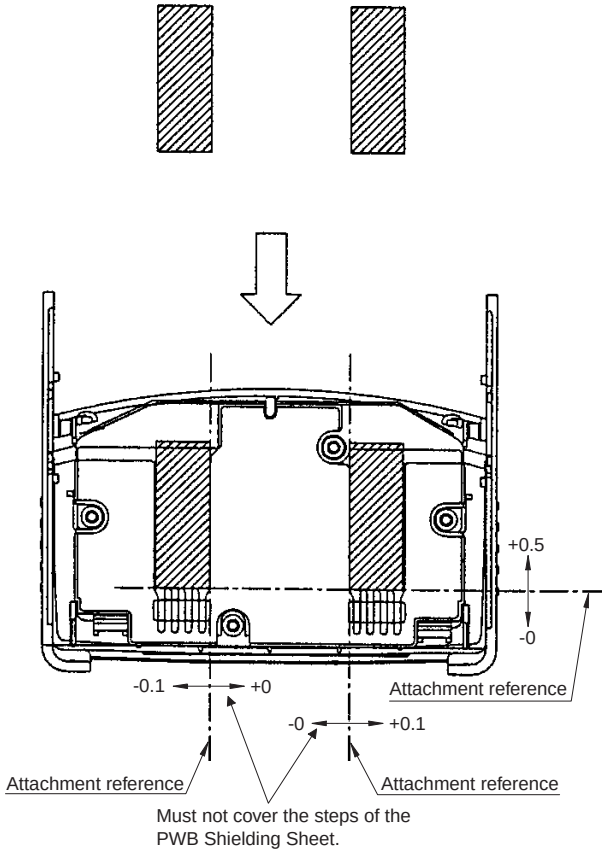
(1) Separate the Sliding Sheet from the Mount Sheet.

(2) Attach the sheet according to the attachment reference of the Shielding Sheet.

Attachment reference: X direction: Inside reference
Y direction: Lead edge of the projection of the Shielding Sheet

(3) After attaching, press the Sliding Sheet along the shape of the Shielding Sheet.

Note: Check that the Sliding Sheet does not cover the Shielding Sheet attachment reference. If it does, push away with a stick, etc.



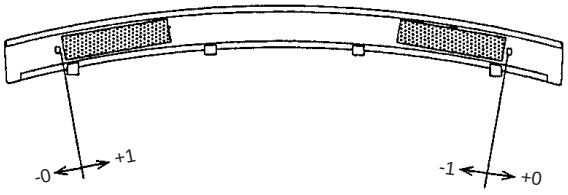
10. Slide Cover Panel Fixing Tape (x 2) attachment

(1) Clean and remove oil with IPA from the Fixing Tape Attachment section of the Slide Cover Panel.

(2) Separate the Slide Cover Panel Fixing Tape from the Mount Sheet.

(3) Attach the Slide Cover Panel Fixing Tape to the Slide Cover Panel.

Note: Attach the tape so that it does not cover the rib.



11. Slide Cover Panel attachment

(1) Clean and remove oil with IPA from the Slide Cover Panel attachment surface of the Slide Cover Cabinet.

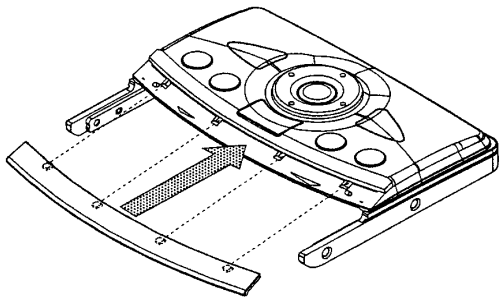
(2) Separate the Slide Cover Panel Fixing Tape from the Separation Sheet.

(3) Assembly the Slide Cover Panel by inserting the Slide Cover Panel Pawls 8x 4) into the Slide Cover Cabinet holes 8x 4).

(4) Press and fix the Slide Cover Panel Fixing Tape.

Note: (1) When pressing and fixing the Slide Cover Panel, do not touch the Key PWB contact surface on the back.

(2) Be sure to separate the Duplex Tape Separation Sheet.



4. UPPER CABINET AND OTHERS DISASSEMBLY AND ASSEMBLY

[NOTE FOR ASSEMBLY OF THE UPPER CABINET UNIT]

1. Tablet Upper Mask attachment

(1) Tablet Upper Mask attachment

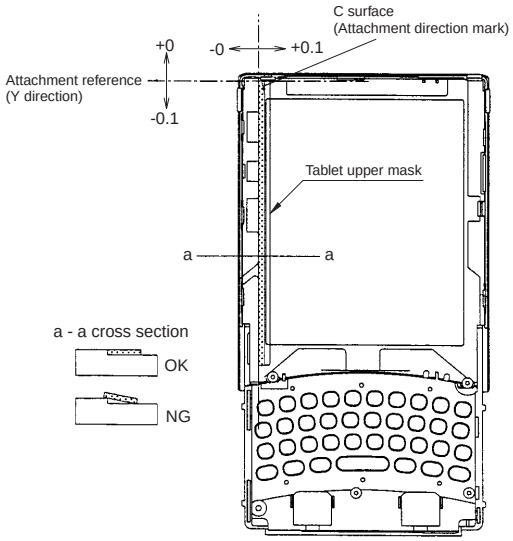
Clean and remove oil with IPA from the attachment section of the Tablet Upper Mask on the back of the Upper Cabinet. Attach the Tablet Upper Mask to the Upper Cabinet along the step on the back with the notch section at the right upper side. After attachment, press the attached section to ensure attachment.

Note: (1) Adhesive is pasted only to the half of the width of the mask. Be careful of the attachment direction.

(2) Attachment deflection reference:

X direction: +0.1mm
–0.0mm (Must not extend over the step.)

Y direction: +0.0mm (Must not extend over the step.)
–0.1mm

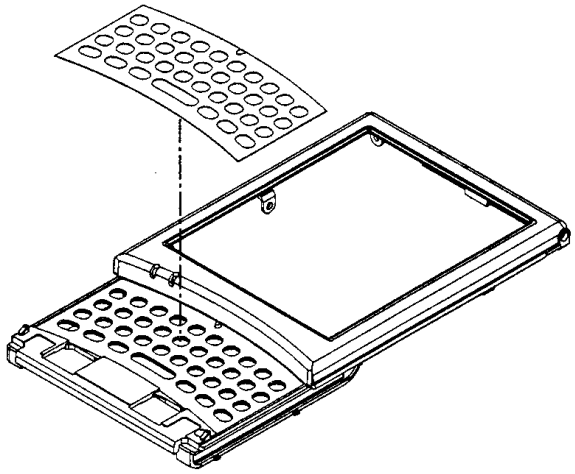


2. Fixing Key Panel attachment

Clean and remove oil with IPA from the attachment section of the Fixed Key Panel of the Upper Cabinet. Attach the Key Panel without extending over the cabinet.

Note: (1) Must not extend over the cabinet.

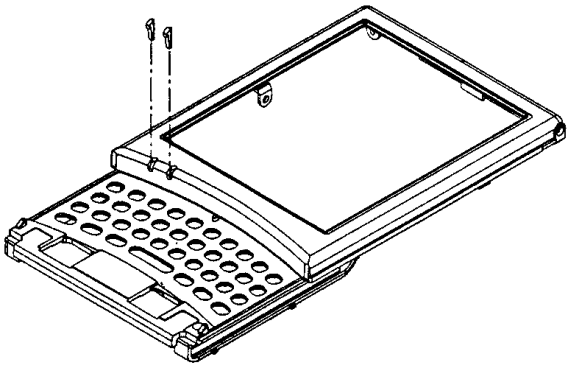
(2) Do not break the pawls when separating the Separation Sheet of the Fixed Key Panel.



3. LED Indicators (x 2) attachment

Insert the LED Indicators (x 2) from the front surface of the Upper Cabinet.

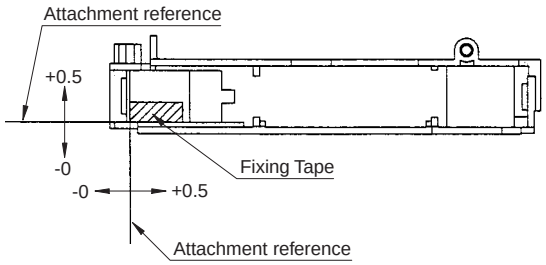
Note: Insert the LED Indicator completely so that it is aligned with the Upper Cabinet.



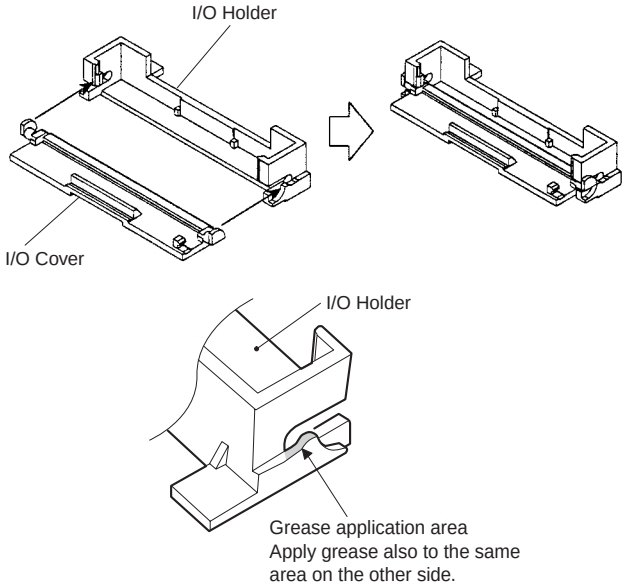
[OTHERS]

1. Inverter Holder Fixing Tape attachment reference

   (1) Attach the Inverter Holder Fixing Tape according to the attachment reference of the Inverter Holder.



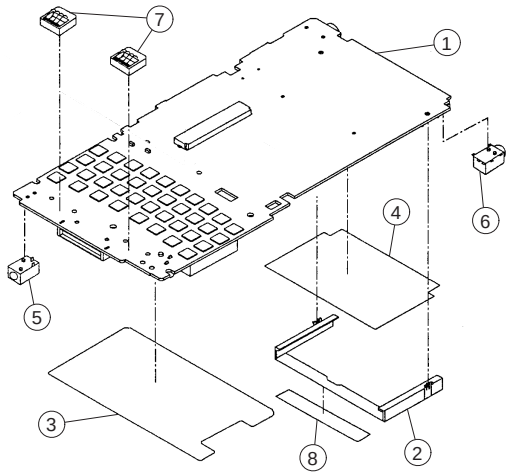
2. Applying grease to the I/O Holder.



5. NOTE FOR THE MAIN PWB UNIT

PARTS LIST

No.	Part name
①	Main PWB Move Unit
②	CF Card Connector Frame
③	Battery Section Insulation Sheet
④	PWB Insulation Sheet
⑤	AC Adapter Jack
⑥	Stereo Headphone Jack
⑦	Contact Spring Unit
⑧	CF Tape



[COUNTERMEASURES AGAINST STATIC ELECTRICITY]

- Use a wrist strap (earth band).
- Never touch the PWB with bare hands.
- When handling the PWB, hold the edge.
- Use only the specified fine solder.
- Soldering condition: 320 degrees, max. 3 sec.

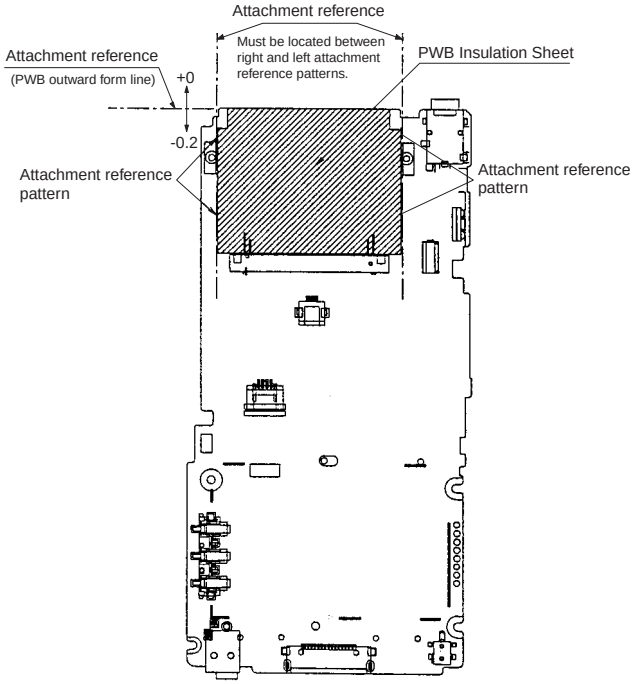
a. PWB Insulation Sheet attachment

Clean and remove oil with IPA from the PWB Insulation Sheet of the PWB, and attach the sheet to the attachment reference. After attachment, press the attached section to secure attachment.

Note: (1) The sheet must not extend out of the outward form of the PWB.

(2) There must be free from wrinkles, folds, and projections by pinching foreign materials.

(3) There must be free from dirt and fingerprints. If there is, remove completely.



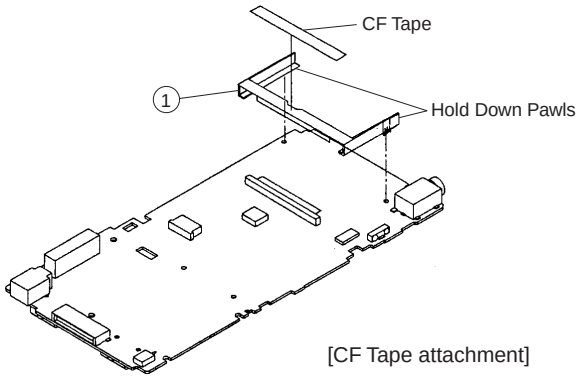
b. CF Card Connector Frame attachment, soldering, CF Tape attachment

While inserting the Hold Down Pawls (2 pcs.) of the CF Card into the PWB, put it over the CF Card Connector. Then solder the Hold Down Pawls (2 pcs.). (Either the front or the back may be soldered.)

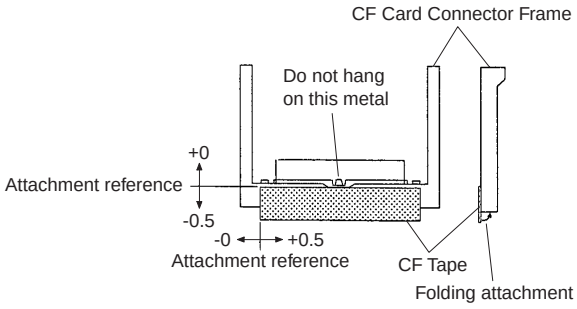
Attach and fold the CF Tape to the CF Card Connector Frame according to the reference below.

Note: (1) Be careful not to bend the CF Connector Pin.

(2) Put the connector frame closely in contact with the PWB.



[CF Tape attachment]



c. Battery Section Insulation Sheet attachment

(1) Clean and remove oil with IPA from the attachment section of the Battery Section Insulation Sheet of the PWB.

(2) Separate the Separation Sheet (small) of the Battery Section Insulation Sheet.

(3) Attach the Battery Section Insulation Sheet to the reference line on the PWB.

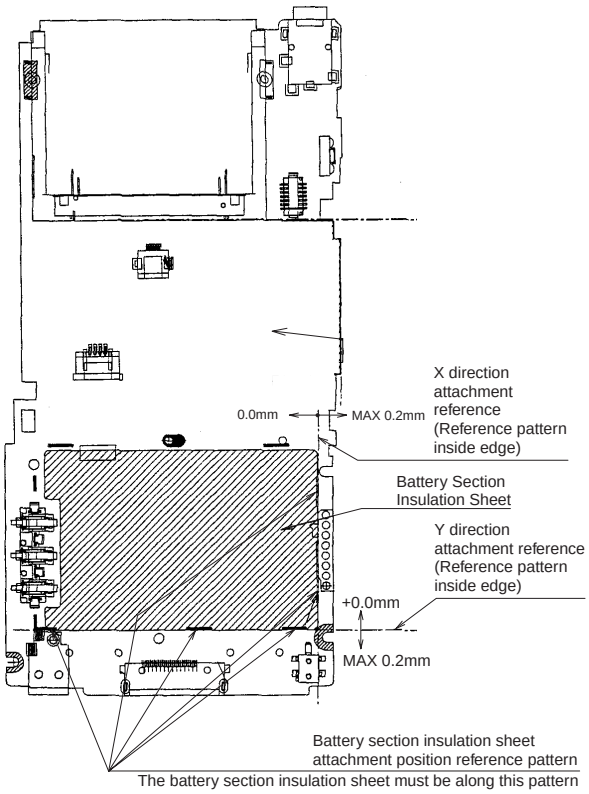
(4) Separate the Separation Sheet (large) and attach the other side.

(5) Press to ensure attachment of the Battery Section Insulation Sheet.

Note: (1) Do not extend out of the reference line.

(2) Must be free from wrinkles, folds, and projections by pinching foreign materials.

(3) Must be free from dirt and fingerprints. If there is, remove completely.


X direction attachment reference (Reference pattern inside edge)
0.0mm
MAX 0.2mm
Battery Section Insulation Sheet
Y direction attachment reference (Reference pattern inside edge)
+0.0mm
MAX 0.2mm
Battery section insulation sheet attachment position reference pattern
The battery section insulation sheet must be along this pattern

d. Stereo Headphone Jack soldering

Insert the positioning ribs (x 2) on the back of the Stereo Headphone Jack into the PWB positioning holes.

Then solder the Stereo Headphone Jack pins (x 6).

Note: If the Stereo Headphone Jack is lifted up, it would make contact with the Lower Cabinet, causing improper engagement of the cabinet. Be sure to make close contact of the Stereo Headphone Jack.

e. AC Adapter Jack soldering **Safety process** ⚠

Insert the positioning ribs (x 2) and pins (x 3) on the back of the AC Adapter Jack into the PWB positioning holes.

Then solder the AC Adapter Jack pins (x 3) from the back of the PWB.

Note: (1) If the AC Adapter Jack is lifted up, it would make contact with the Lower Cabinet, causing improper engagement of the cabinet. Be sure to make close contact of the AC Adapter Jack.

(2) If pins should be shorted, heat or smoke would be generated. Use great care not to short the solders.

f. Contact Spring Unit (x 2) soldering

Insert the positioning ribs (x 2) on the back of the Contact Spring Unit into the PWB positioning holes. After insertion, solder the Contact Spring Unit Pins (x 4).

Note: (1) If the Contact Spring Unit is lifted up, it would make contact with the Lower Cabinet, causing improper engagement of the cabinet. Be sure to make close contact of the unit and the PWB.

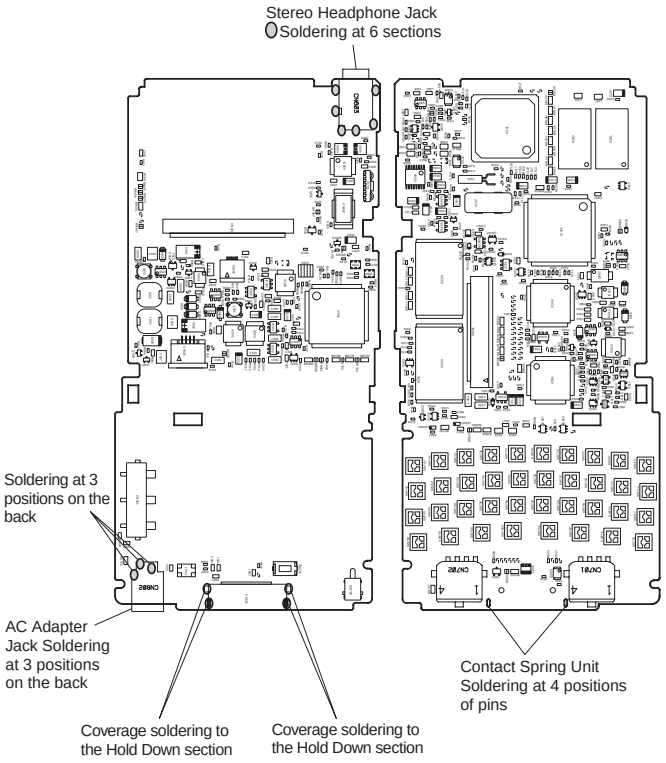
(2) Be careful not to allow adhesion of solder to the contact spring or deform of the spring, or the Slide Cover Contact may be improperly connected. (Do not use a part with adhesion of solder or deformed part.)

g. 16pin Connector Coverage Solder

Perform coverage soldering to the left and right Hold Down sections (4 positions) of the 16Pin connector.

Note: (1) Soldering conditions: 350 degrees, within 3sec

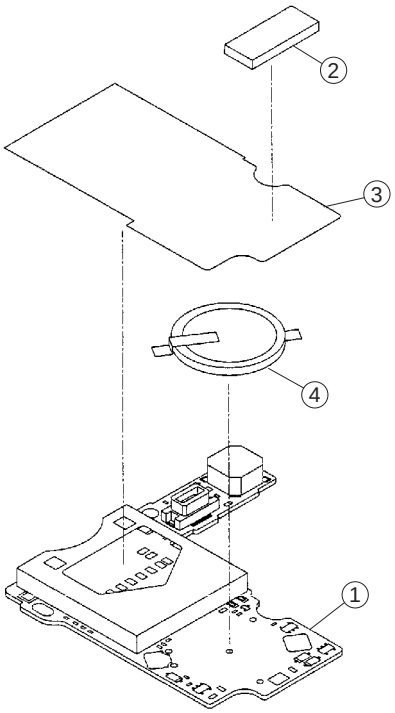
(2) Avoid square soldering and improper soldering.


Stereo Headphone Jack Soldering at 6 sections
Soldering at 3 positions on the back
AC Adapter Jack Soldering at 3 positions on the back
Contact Spring Unit Soldering at 4 positions of pins
Coverage soldering to the Hold Down section
Coverage soldering to the Hold Down section

6. NOTE FOR THE SUB PWB UNIT

PARTS LIST

No.	Part name
①	Sub PWB Unit
②	Back Up Battery Cushion
③	Back Up Battery Insulate Sheet
④	Litume Battery



1. Back Up Battery soldering **Safety process**

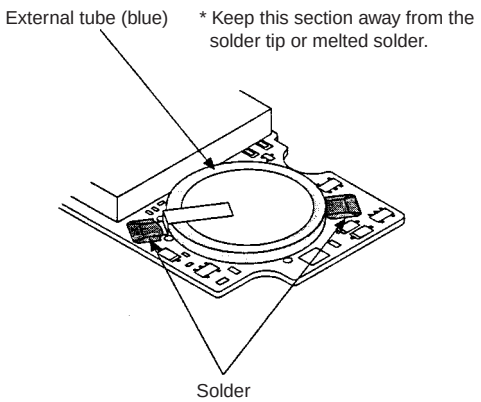
   (1) Solder the two terminals of the Back Up Battery firmly with the PWB. (Be careful of the polarity.)

   Soldering conditions: 250°C ~ 300°C, within 5 sec

   If the battery is once soldered improperly, it cannot be used for ever. (Never use it.)

   The solder tip or melted solder must be kept away from the external tube (blue) of the battery. If they are brought into contact,

   the battery will be shorted. Especially if the tube under the negative (–) terminal is melted, the positive (+) terminal and the negative (–) terminal will be shorted.



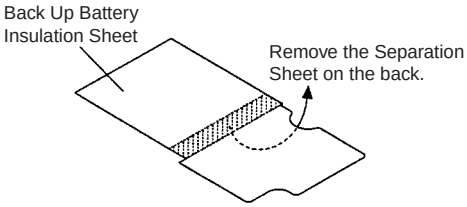
Never put a circuit board on another or never put it on a metal surface.

2. Back Up Battery Insulation Sheet attachment **Safety process**

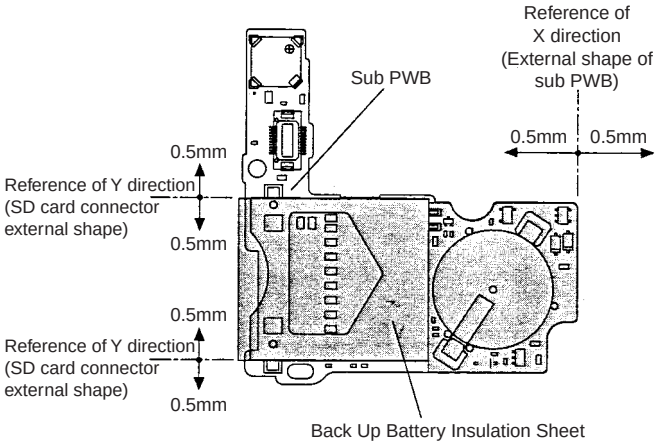
   (1) Remove the separation sheet from the back of the Back Up Battery Insulation Sheet. (Partial paste)

   (2) Attach the Back Up Battery Insulation Sheet to the SD card so that it fits with the external shape of the sub PWB.

   - If the Back Up Battery Insulation Sheet is broken or if it is not attached, the battery will be heated to smoke. Use great care to avoid it.
   - The Back Up Battery Insulation Sheet must not extend out of the external shape of the sub PWB.



<Back Up Battery Insulation Sheet attachment reference>

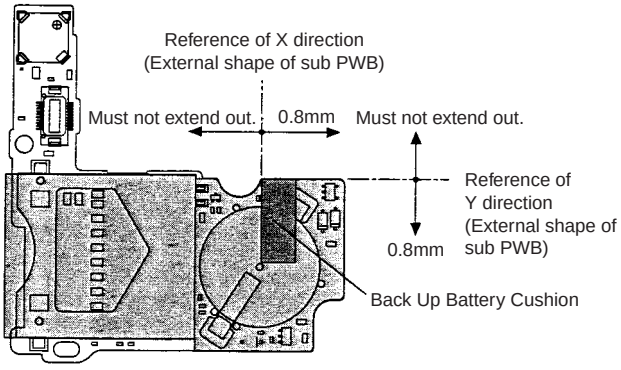


3. Back Up Battery Cushion attachment

   Attach the Back Up Battery Cushion according to the attachment reference shown below.

   - The Back Up Battery Insulation Sheet must not extend out of the external shape of the sub PWB.

<Back Up Battery Cushion attachment reference>


Reference of X direction (External shape of sub PWB)
Must not extend out.
0.8mm
Must not extend out.
Reference of Y direction (External shape of sub PWB)
0.8mm
Back Up Battery Cushion

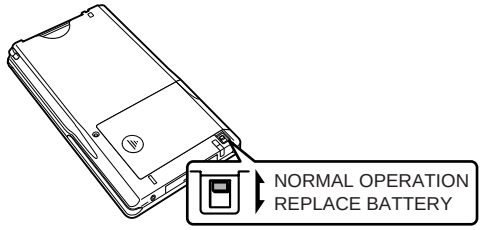
CHAPTER 4. NOTES FOR SERVICING

1. RESETTING THE DEVICE

(1) SOFTWARE RESET

A strong impact, exposure to an electrical field, or other unusual conditions may render the SL-5500 inoperative. Pressing the keys may have no effect. If this occurs, follow the instructions below.

1. Set the Battery Replacement Switch to the “REPLACE BATTERY” position and then back to “NORMAL OPERATION”.
2. Press [Cancel] (On/Off) to restart the SL-5500. The Home screen will be displayed.

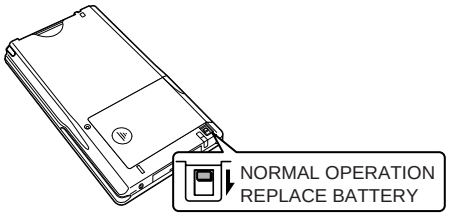


(2) HARDWARE RESET

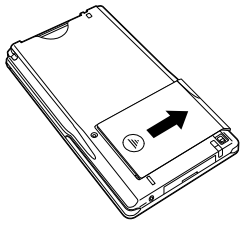
If the SL-5500 still fails to function after the software reset is done shown above, you will have to do hardware reset.

Caution:Performing the hardware reset will erase all data created and all add-on applications installed in the SL-5500.

1. Slide the Battery Replacement Switch on the rear side of the unit to the “REPLACE BATTERY” position.

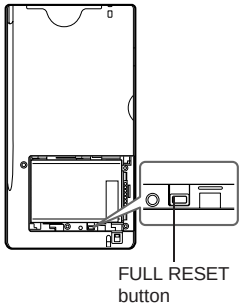


2. Open the Battery Compartment Lid.



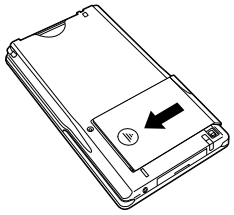
3. Push “FULL RESET” button (2~3 seconds) on the lower right side of the battery compartment with the Stylus.

Note: Do not use an object with a breakable or sharp tip.



4. Replace the Battery Compartment Lid.

Note: Be sure to replace the Battery Compartment Lid before you use.



5. Slide the Battery Replacement Switch to the “NORMAL OPERATION” position.
6. Press [Cancel](On/Off) to turn the power ON.

   The Welcome screen appears.

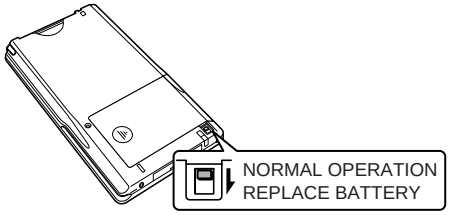
   Then, follow the next procedures to complete the initial settings.

   - Adjusting the touch panel.
   - Setting the date and time.
   - Registering your personal information.
   - Setting your pass code.

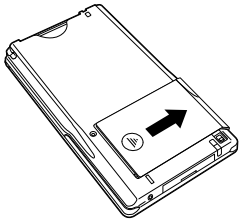
Note:
- If the Welcome screen doesn’t appear, try FULL RESET again. Also check the Battery Replacement Switch is set to “NORMAL OPERATION” and battery is inserted correctly.
- If the battery level is low, the power will not turn on even if you attach the AC adapter. Charge the battery to its full capacity.

2. TO INSERT THE BATTERY

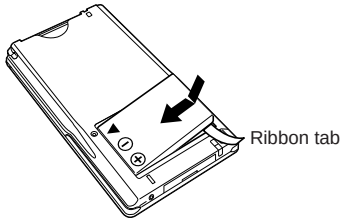
1. Slide the Battery Replacement Switch on the rear side of the unit to the “REPLACE BATTERY” position.



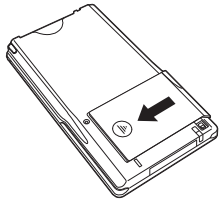
2. Open the Battery Compartment Lid, and gently pull it off.



3. Insert the battery on the ribbon tab, making sure that the triangle (◀), plus (+), and minus (-) marks on the battery are aligned correctly with those printed inside the battly conpartment.



4. Replace the Battery Compartment Lid with the ribbon tab inside.



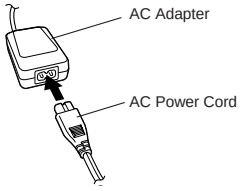
Note: Be sure to replace the Battery Compartment Lid after inserting the battery.
If the cover is not on securely, the battery may become loose and you may lose the data stored in the unit.

5. Slide the Battery Replacement Switch to the “NORMAL OPERATION” position.
When you use the battery for the first time, charge the battery.

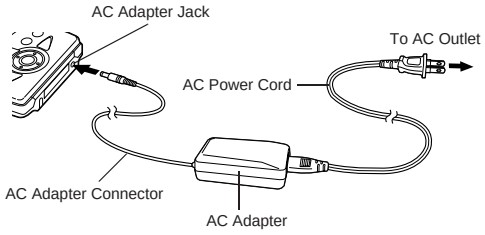
3. CHARGING

Note: Only use “EA-70” AC Adapter (supplied).

1. Connect the AC Power Cord to the AC Adapter.



2. Plug the AC Adapter connector into the SL-5500 which contains the battery as shown to the below.



3. Plug the AC Power Cord into an AC Outlet.
The LED indicator on the unit (Charge Light) will turn amber when charging begins.
Standard charging time: Approx. 2.5 hours (depending on the temperature and usage conditions).

4. When the charging has been completed, the LED indicator will turn off. Unplug the AC Power Cord from an AC Outlet, then unplug the AC Adapter Connector from the SL-5500.

Notes:
- Charge the battery to its full capacity until the LED indicator turns off.
- If a charging error occurs, the LED indicator will flash. Make sure that the AC power cord and the AC adapter are connected correctly, remove and reinsert the battery, then perform steps 1 to 3 above again. If the error persists, there is something wrong with the battery, SL-5500, etc.
- The AC power cord plug may differ in some countries.

The SL-5500 has a specified built-in rechargeable back-up battery that prevents the memory contents from being erased when you replace the battery.
The rechargeable back-up battery will be charged to its full capacity in 30 hours using the AC adapter or a fully charged "EA-BL06" operating battery. If you want to replace the operating battery before the rechargeable back-up battery is fully charged, be sure to connect the AC adapter.

4. WRITING BOOT PROGRAM USING JTAG

If the boot program which changes the internal flash memory of the SL-5500 won’t start, update the boot program using the procedure given below.

[NECESSARY TOOLS]

- JTAG cable [PARTS CODE:0IU-PLGWB9727]
- Flash Memory Write Program (Supplied by Sharp)
- PC
- Windows 95/98/NT4.0/2000
- Parallel terminal for bi-directional communication.
- SL-5500

1. Install the “Flash Memory Write Program” into the PC.

   Install the program into the JTAG write PC, referring to Readme.txt in the program supplied by Sharp.

   The Readme.txt may contain the latest information, which is not covered in this document.

2. Remove the Main Battery and AC Adapter from the SL-5500.

   After few minutes, then attach the Main Battery and AC Adapter and press and hold the FULL RESET button down for a few seconds.

3. Connect the PC’s parallel port and the SL-5500 with the JTAG cable.

4. Start the command prompt on the PC.

   Move to the folder where the above program was unpacked, using cd command.

5. Hold the FULL RESET button down for a few seconds.

6. Execute ‘update.bat’ in the folder.

   As for Flash Memory Write Program, CPU can perform under operation.

   Immediatery after FULL RESET, CPU surely comes during operation.

   Please perform ‘update.bat’ immediately after FULL RESET.

7. Writing starts and the progress message is displayed.

   If writing does not start and an error occurs, check that the JTAG cable is properly connected.

   If not, remove the Main Battery and AC Adapter from the SL-5500 and repeat the procedure again.

8. If the following message appears on screen, writing has been normally completed.

   “Verification successful!” is displayed twice.

progress messages

J:¥JTAG5500>update

J:¥JTAG5500>jflash BOOTSHP2.bin

JFLASH Version Special CPU only (no CPLDs) 1.2 for SHARP Flash SA-1110 revision B4

Number of blocks in device = 256

Block size = 32768 0x8000

Device size = 16777216 0x1000000

Unlocking block 0

unblock OK

Starting erase

Erasing done

Starting programming

Programming done

Starting verify

Verification successful! ← Check

J:¥JTAG5500>jflash cf.bin P 1

JFLASH Version Special CPU only (no CPLDs) 1.2 for SHARP Flash SA-1110 revision B4

Number of blocks in device = 256

Block size = 32768 0x8000

Device size = 16777216 0x1000000

Unlocking block 1

unblock OK

Starting erase

Erasing done

Starting programming

Programming done

Starting verify

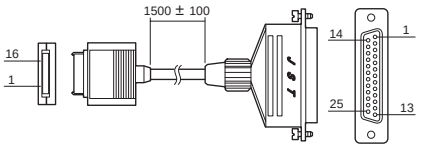
Verification successful! ← Check

9. When the second “Verification successful!” is displayed, the writing is finished.

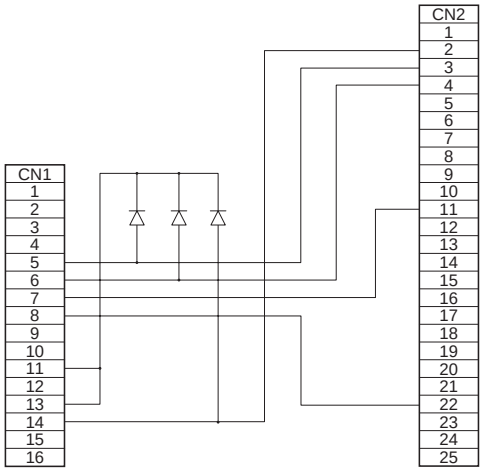
Note: If you cannot exit the program successfully, remove the Main Battery and AC Adapter from the SL-5500 and repeat the above procedure.
If you cannot exit the program successfully again, it is suggested that SL-5500’s JTAG I/F or Internal Flash Memory is defective.

10. If you can exit the program successfully, then install the latest software from the web site.
(Refer to 5. INSTALLING PROCEDURES OF THE LATEST SOFTWARE)

[JTAG CABLE CONNECTION DIAGRAM]



※PARTS CODE: OIU-PLGWB9727



5. INSTALLING PROCEDURES OF THE LATEST SOFTWARE

Install the latest software after completion of repair as follows:

1) Prepare PC card type CF card adapter with CF FROM card (64MB).
2) Download the latest updated software file (zip file) from the web site (http://developer.sharpsec.com).
3) Unzip the zip file on PC. “OSPACK” file will be created.
4) Copy the file to the root directory of the CF card.
5) Insert the CF card to the SL-5500.
6) Connect the AC Adapter to the SL-5500.
7) Open the Battery Compartment Lid. Press the FULL RESET button while pressing “C” key and “D” key.
8) The green and orange LED will turn on, and updating the Flash ROM in the device will start.

   Caution: Please don’t abort or remove the AC Adapter until the LED is turned off.
9) After about 3 minutes, the green and orange LED will turn off. (Updating the Flash ROM is finished.)
10) Remove the CF card, and press FULL RESET button.
11) Close the Battery Compartment Lid, and set the Battery replacement switch to “NORMAL OPERATION” position.
12) Press On/Off key. Then the System will start.

6. CAUTION

When the boot program is written or the flash ROM (IC203,IC204) is replaced, the following setup should be executed, after downloaded the latest software from web site.
Boot the diag and execute the following setup referring to the Service manual.

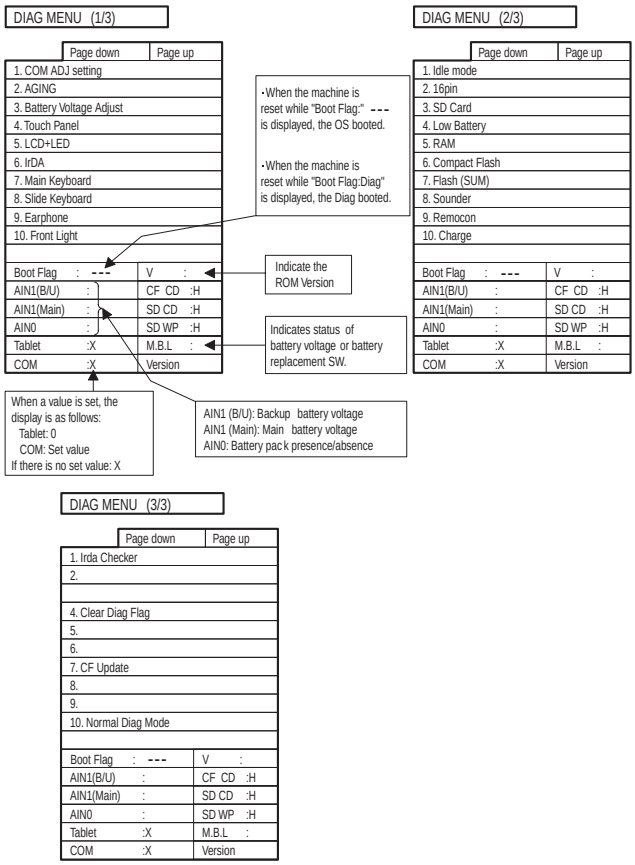
① Display density adjustment, writing (Page 54)

② Touch panel adjustment procedure (Page 55)

CHAPTER 5. DIAGNOSTICS AND CHECK ITEMS

When diag are executed, data of user will be cleard.
If you need the data, you must transfer the data before starting diag.

1. DIAG MENU



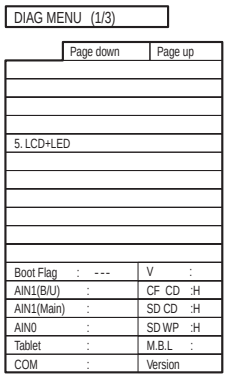
Entering the DIAG mode: Press and hold [P] and [D] keys, and press FULL RESET button simultaneously.

Key operations

Slide key	Main key	Operation	
Cancel (on/off)		Turns on the power.	
Cursor upper	A	Shifts the selected menu item upward.	Effective only on the menu display.
Cursor lower	D	Shifts the selected menu item downward.	Effective only on the menu display.
Cursor right	B	Refer to the next page	Effective only on the menu display.
Cursor left	L	Refer to the previous page.	Effective only on the menu display.
OK	ENTER	Starts the selected check	
Cursor key center	←	Interrupts the check under process and returns to the menu.	
Contact + OK	Fn + ENTER	Writes the set value while the common voltage is being adjusted.	
Front Light		Turns on/off the Front Light. (Toggle operation)	
	1,2,.....9,0	Selects and execute the menu.	Effective only on the menu display.

When the Normal Diag Mode (Diag Menu (3/3) No. 10) is executed, if “Full reset” is made, the diag is booted.
To boot the OS, execute Clear Diag Flag (Diag Menu (3/3) No.4).

LCD/LED CHECK



Note : The display must be free from unevenness and flicker.

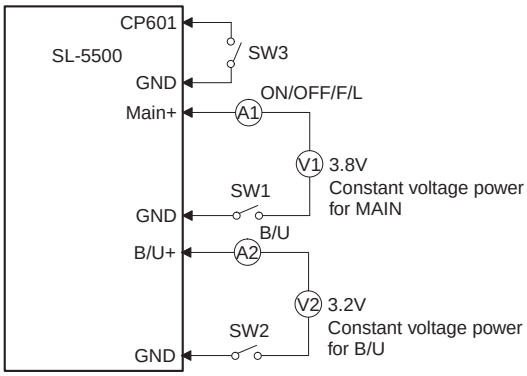
○: ON ×: OFF F: Flashes

F/L: Front Light

No.	Operating procedure	Display	LED		F/L	Check item
			Orange	Green		
1	Connect the AC adapter, supply power to the SL-5500, and press the FULL RESET button.	DIAG MENU (1/3)	×	×	×	DIAG is booted.
2	Touch No. 5 LCD + LED.	White background	×	×	MAX	White background is displayed. F/L turns on.
3	Press [OK] key.	White background	×	×	×	White background is displayed. F/L turns off.
4	Press [OK] key.	White background	×	×	MIN	White background is displayed. F/L turns on.
5	Press [OK] key.	Gradation	×	×	2nd	Black on the lower side and white gradually increases as it goes up.
6	Press [OK] key.	Black/white one-point check pattern	×	×	3rd	Check pattern. F/L is rather bright.
7	Press [OK] key.	Black/white one-point check pattern	×	×	MAX	Check pattern. F/L is rather bright.
8	Press [OK] key.	Black background	○	×	MAX	Black background (Ignore bluish color.) Orange LED turns on.
9	Press [OK] key.	Red background	×	○	MAX	Red background Green LED turns on.
10	Press [OK] key.	Green background	○	○	MAX	Green background Both LED's turn on.
11	Press [OK] key.	Blue background	F	F	MAX	Blue background Both LED's flashing.
12	Press [OK] key.	DIAG menu	×	×	×	Enters DIAG menu. Both LED'S/FL's turn off.
13	Press [on/off] key.	Turns off.	×	×	×	After the display turns off completely

CURRENT CONSUMPTION CHECK

No.	Operating procedure	Display	Check item
1	Check that the SL-5500 battery replacement switch is locked.		
2	As shown in Fig-1, supply power to the SL-5500. V1 = 3.8V Boot the diag mode (SW1~SW3 = ON)	DIAG MENU (1/3)	
3	Touch the [Page up], Select No. 1 Idle mode of DIAG MENU (2/3)	Idle mode	ON current (A1) = 160mA or less
4	Press [F/L] key of the SL-5500.	DIAG MENU (1/3) F/L ON	F/L current (A1) = 550mA or less
5	Press [on/off] key once to turn off the power.	(turn off)	OFF current (A1) = 1mA ~ 2.75mA
6	Supply power of 3.2V to the backup battery side. V2 = 3.2V (V1 = 0V (SW1 = OFF)), (SW3 = OFF)		B/U current (A2) = 1mA ~ 2.5mA



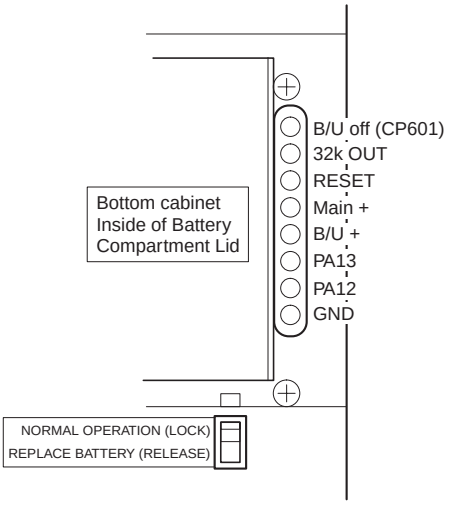
Main battery supply voltage = 3.8V

Backup battery supply voltage = 3.2V

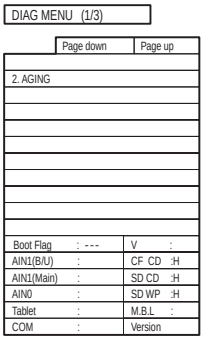
(Note for measurement of currents of backup and main batteries.)

- When measuring the current, short CP601 and GND.

CHECK PAD

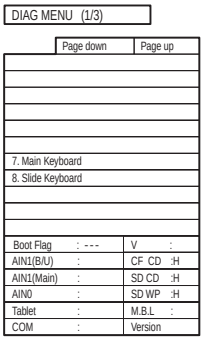


RAM CHECK



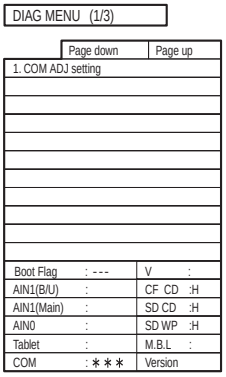
No.	Operating procedure	Display	Check item
1	Connect the AC adapter to supply power to the SL-5500, and boot the diag.	DIAG MENU (1/3)	
2	Shift the cursor down.	DIAG MENU (1/3)	
3	Select No. 2 AGING.	FLASH CHECK SUM → RAM CHECK → LCD CHECK → ALARM CHECK → RAM CHECK	Aging starts up. (LED turns on at every check.) FLASH CHECK : Green RAM : Orange LCD : Green ALARM : Orange RAM : Orange
4	Check operations.		Check that the above check is repeated twice or more. If the check operation is stopped, it is NG.
5	Press the cursor center key.	DIAG MENU (1/3)	

KEYBOARD CHECK



No.	Operating procedure	Display	Check item
1	Connect the AC adapter to supply power to the SL-5500, and press FULL RESET button to boot the DIAG menu.	DIAG MENU (1/3)	
2	Select No. 8 Slide Keyboard.	Press Activity key.	
3	Shift the slide key down.	Press Activity key.	
4	Press keys according to the display. [Activity] [Contacts] [Home] [Menu] [Mail] [Cancel] [Up] [OK] [Left] [Center] [Right] [Down]		OK is displayed. (Not NG)
5	Press [OK].	DIAG MENU (1/3)	
6	Select No. 7 Main keyboard.	Press Q key.	
7	Press keys according to the display.		OK is displayed. (Not NG)
	[Q] [W] [E] [R] [t] [y] [U] [I] [Q] [p] [A] [S] [D] [F] [G] [H] [J] [K] [L] [←] [↑] [Z] [X] [C] [V] [B] N] [M] [;] [↑] [Fn] [Tab] [/?] [Space] [‘ “] [. :] [ENTER]		
8	Press [OK] key to return to the menu.	DIAG MENU (1/3)	
9	Press [on/off] key to turn off the power.		
10	After the display is turned off completely, disconnect the AC adapter.		

DISPLAY DENSITY ADJUSTMENT, WRITING

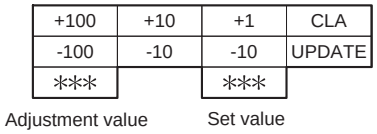
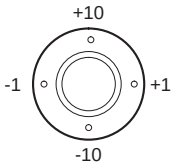


(Environmental conditions for display density adjustment, setting)

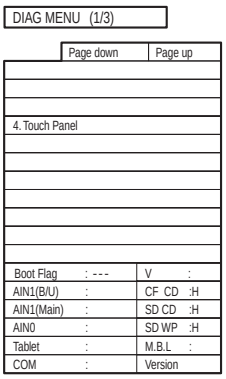
Kind of power source: Inverter fluorescent lamp (3-wavelength daytime white)

Panel surface illumination: 2500 ± 500 lx

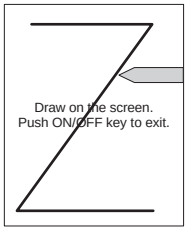
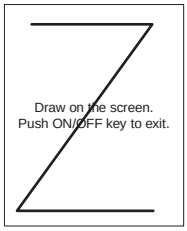
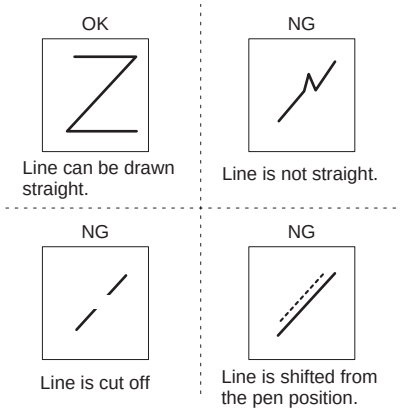
Ambient illumination: 300 ~ 700 lx

No.	Operating procedure	Display	Check item
1	Connect the AC adapter to supply power to the SL-5500. Press FULL RESET button to boot the DIAG mode. If the DIAG is not booted by pressing FULL RESET button, press and hold [P] + [D] and press FULL RESET button simultaneously.		
2	Press Front Light key to turn on the light.	DIAG MENU (1/3)	Front Light turns on.
4	Press [OK] key.		
5	Check for the set value which provides no flicker of display with the cursor key.		There is no flicker of display.
6	Remember the adjustment value of the display, and press [UPDATE] of tablet.	DIAG MENU (1/3)	COM: ✶✶✶✶✶ becomes the set value.
7	Press Front Light key to turn off the light.	DIAG MENU (1/3)	F/L turns off.
8	Press [on/off] key to turn off the power. After the display is turned off completely, disconnect the AC adapter.		

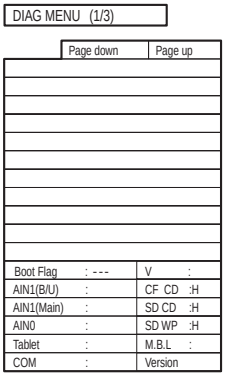
TOUCH PANEL ADJUSTMENT PROCEDURE



Note: Check by viewing from right above the center of the display.

No.	Operating procedure	Display	Check item
1	Connect the AC adapter to supply power to the SL-5500, and press FULL RESET button to boot the DIAG menu.	DIAG MENU (1/3)	
2	Press Front Light key to turn on the light.	DIAG MENU (1/3)	
3	Select No. 4 Touch Panel.	Touch Panel Menu 3. Touch Calibration 4. Scribble	
4	Press [OK] key. (Select Touch Calibration.)	Touch panel adjustment screen	
6	Touch two marks “+” for 1sec or more. At that time, the value is written into the Flash ROM.	White background	The marks “ + “ are changed to red.
7	 Draw lines with the attached pencil at a normal strength of writing.		
8	Press [on/off] key and press [cursor center] key.	DIAG MENU (1/3)	
9	Press [on/off] key. After the display is turned off completely, disconnect the AC adapter.		

SOFTWARE VERSION CHECK PROCEDURE



No	Operating procedure	Display	Check item
1	In DIAG MENU (1/3), touch “Version” at the right lower section of the display.		Version List CPU:SA1110 B4 (or SA1110B5) Board: 01 ROM: USA ∗ . ∗∗ (Version) ROM:C.S.: ∗∗∗∗ (Check sum)
2	Press the center key of the cursor to return to the menu.	DIAG MENU (1/3)	
3	Press [on/off] key to turn off the power. After the display is turned off completely, remove the Main battery.		

CONFIRMATION PROCEDURES OF CF CARD / SD CARD / STEREO HEADPHONE JACK

1. Prepare a CF card (or SD card) and MP3 music data.
2. Reproduce the music data with an application (Media Player) and check it with the stereo headphone.

∗ To check the CF card or SD card in the diag mode, a special tool is required. Therefore this confirmation is made on the OS and an application.

2. TEST PROCEDURES OF SL5000 / SL5500 I/O PORTS

1) IRDA PORT TEST

Test by Diag/Target SL5500 or SL5000

	Test target SL5500	Checker SL5500
1		Enter the diag mode. (Push and hold "P" and "D", and push Full Reset at the same time.)
2		Use the cursor key to open "DIAG MENU (3/3)" .
3		Tap "No.1 IrDA Checker."
4	Open "DIAG MENU (1/3)" .	
5	Face the IrDA port of the target SL-5500 toward that of the checker SL-5500.	
6	Tap "No.6 IrDA." === IrDA check Slave === Push [On] button to menu 1 checking ... OK ←If "OK" is indicated, transmission is performed normally. This figure will count up if the operation is performed normally.	

2) TEST PROCEDURES OF STEREO HEADPHONE/MICROPHONE/SOUNDER

Test by Diag

1	Open "DIAG MENU (1/3)".			
2	Connect a stereo headphone or a speaker with amplifier to the stereo headphone jack. (Do not put the stereo headphone in the ears because it produces too big sounds.)			
3	Tap "No.9 Earphone."			
		Operation	Display	Test content
	①	Check the display on the right.	Audio Sampling	Recording test (Outputs from stereo L-ch, loops in the PWB to microphone input)
			↓	
	②		Audio Out Left	Stereo Headphone Jack L-ch test (Recorded data above are outputted.)
		Press "OK" key.	↓	
	③		Audio Off	
		Press "OK" key.	↓	
	④		Audio Out Right	Stereo Headphone Jack R-ch test ((Recorded data above ① are outputted.)
		Press "OK" key.	↓	
	⑤		Audio Muting	Mute circuit (Q605-related) - Test for no sound
		Press "OK" key.	↓	
	⑥		Audio Volume Check	Volume (IC301/IC604) - Test of step-by-step variations in sound volume
		Automatic	↓	
			MonoAudio Check	Recorded data ① are outputted from ANALOG OUT (IC501) .:Sub PWB's sounder sounds.
		Press "OK" key.	Returns to the menu by "OK" key.	
				Execute the above test and check the actual sounds.

3) SD CARD SLOT TEST

Test by OS

1 Prepare data in the built-in memory of the machine.
MP3 music data will be OK.

2 Insert an SD card.

Check that the SD card icon is indicated on the task bar.

If the SD card icon is not indicated on the task bar, remove the SD card and insert it again and check the icon.

3 Copy the data in the machine to the SD card.

4 If copying is performed normally, it is OK.

For operating procedures, refer to the Operation Manual.

4) USB PORT TEST (SOME OF SHARP I/O PORTS (16PIN CONNECTOR))

Test by OS

1 Preparation

Docking Station

Personal computer with USB support (Win98 or later)
(The USB driver and necessary application must have been installed to the computer from the CD-ROM packed together with the machine.)

2 If synchronization and data transmission are performed normally, it is OK.

For operating procedures, refer to the Operation Manual.

SL5500: Use Docking Station (CE-ST7).

SL5000: Use Docking Station (CE-ST6).

5) SERIAL PORT TEST (SOME OF SHARP I/O PORTS (16PIN CONNECTORS))

1. Control line test

Test by Diag

Test jig: Use the following circuit. (Prepare it on each service spot.)

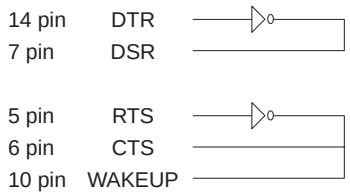
1 Open "DIAG MENU (2/3) ".

2 Connect the following test circuit.

3 Tap "No1 16pin."

Display

=== 16pin Test ===
16pin test Complete
Hit any key to continue
----Status messages----
OK ← Check that "OK" is indicated.

Test circuit	Test content	Check content
 Note: Supply this IC power from VCC-GND of 16in connector. ic:74HC14 or 74HC04	① Make RTS="H". Make DTR="L".	Check that CTS="L" Check that WAKEUP="H" Check that DSR="H"
	② Make RTS="L". Make DTR="L".	Check that CTS="H" Check that WAKEUP="L" Check that DSR="H"
	③ Make RTS="L". Make DTR="H".	Check that CTS="H" Check that WAKEUP="L" Check that DSR="L"
	④ Make RTS="H". Make DTR="H".	Check that CTS="L" Check that WAKEUP="H" Check that DSR="L"

2. Data line test

Test by Diag

Test jig:CE-170TS PC (with RS-232 (9pin) support)		The terminal adapter confirmed by Technical Division is Tera Term (Pro) (Free software of terminal emulator (communication program) .)		
	SL5500	PC		
1		Connect the CE-170TS, and boot the terminal adapter.		
2		Terminal adapter setup	Speed	2400 (bps)
			Parity	None
			Data length	8bit
			Stop bit	1bit
			Xon/Xoff	Not used
			Shift in/out	Not used
3	Push and hold "R" and "D", and push Full Reset at the same time.	The PC's display indicates "READY REMOTE CHECK."		
4		Enter "RA" in caps. If entered in small letters, "raNG Command error" is displayed.		
5	SL5500 displays as follows: Alarm Check Wait 1s OK			
6		The screen displays as: RAOK		
7	Execute Full Reset. Remove the CE170TS.			

Note: When "R" + "D" keys and Full Reset are pushed at the same time, the machine enters the test mode.
Be careful no to touch the keys of PC at that time.

6) CF CARD SLOT TEST

Test by Diag

Test jig:Use "CF test 220" of SYCARD Technology.

1 Open "DIAG MENU (2/3)"

2 Install the AC Adapter (EA-70) and the SYCARD (CFtest220).

3 Tap "No.6 Compact Flash".

Display

CF Connector Check

----- Status messages------

Test procedure

0. CD1#, CD2#
1. Data 15-8, REG#, WE#, RD#
2. Data7-0, CE1#
   IOWR#, IORD#, WAIT#
3. AddressBus A10-A0, CE1#, CE2#, OE#
4. VCC, BVD1, BVD2, WP, RDY
5. VS1, VS2

At last, if the display indicates as below, it is OK.

----- Status messages-----

CHAPTER 6. TROUBLE SHOOTING

CONTENTS

1. DOES NOT OPERATE
2. DOES NOT DISPLAY (THERE ARE KEY SOUNDS, BUT NO DISPLAY.)
3. THE FRONT LIGHT DOES NOT TURN ON
4. INPUT OPERATIONS WITH THE TABLET ARE INVALID
5. CANNOT BE DISCHARGED
6. KEY INPUTS ARE INVALID
7. ABNORMAL DISPLAY COLORS
8. SHORT BATTERY LIFE
9. THE CF CARD (SD CARD) IS NOT RECOGNIZED. / WHEN THE CF CARD IS INSERTED, NO OPERATION IS PERFORMED

Note: 1. When receiving a repair request, explain that user data are not recovered.

If recovery of user data is strongly requested, try to backup only the PIM data without warranty.

(For the utility program, use one that is supplied from Sharp.)

2. Check that the program in the FLASH ROM is what was released by Sharp.

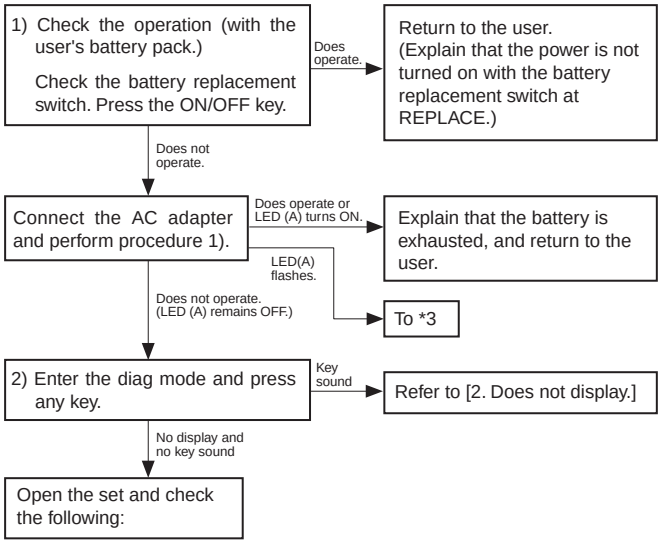
(If the program has been modified by the user, it may be out of warranty.)

3. When the machine enters the diag mode, the user data are destroyed.

When checking with the diag, be sure to confirm the user whether the user data should be recovered or not in advance.

If the user data should be recovered, back up the user data before executing the diag operations.

1. DOES NOT OPERATE


1) Check the operation (with the user's battery pack.)
Check the battery replacement switch. Press the ON/OFF key.
Does operate.
Return to the user. (Explain that the power is not turned on with the battery replacement switch at REPLACE.)
Does not operate.
Connect the AC adapter and perform procedure 1).
Does operate or LED (A) turns ON.
Explain that the battery is exhausted, and return to the user.
LED(A) flashes.
Does not operate. (LED (A) remains OFF.)
To *3
2) Enter the diag mode and press any key.
Key sound
Refer to [2. Does not display.]
No display and no key sound
Open the set and check the following:

1) Check the voltage of each power source.

- Is VCC3 normal? VCC3=3.3V ± 0.3V
- Is VCC5 normal? VCC5=5V ± 0.5V
- Is VCC-CORE normal? VCC-CORE=1.8V ± 0.18V

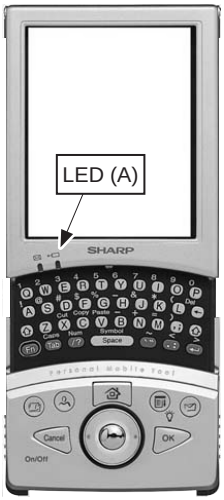
2) Check for disconnection of the fuse in each power line.

- Fuses to be checked: "F803" "F806" "F805" "F801"

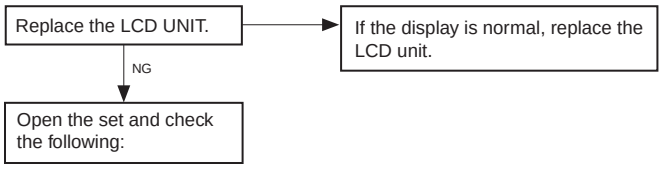
  Check conduction with a tester. (Be careful to avoid contact between the tester probe and the parts.)

*3: Check the figure of AIN0 that is displayed on the lower side of the diag menu.

- If the figure is 1000 or greater, it might be considered that no battery is inserted.
- Replace the battery with new one.



2. DOES NOT DISPLAY. (THERE ARE KEY SOUNDS, BUT NO DISPLAY.)

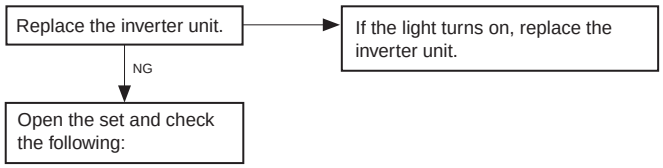


∗Enter the diag mode and check the following.

1) Check the voltage levels related to the LCD.
: +15V (TP357) = +15V ± 5%
: -15V (TP350) = -15V ± 5%
: -12V (TP356) = -12V ± 1V
: VSHA (TP318) = +5V ± 10%
: VSHD (TP308) = +3.3V ± 10%

2) Check that the FPC of LCD is properly connected to the connector.

3. THE FRONT LIGHT DOES NOT TURN ON



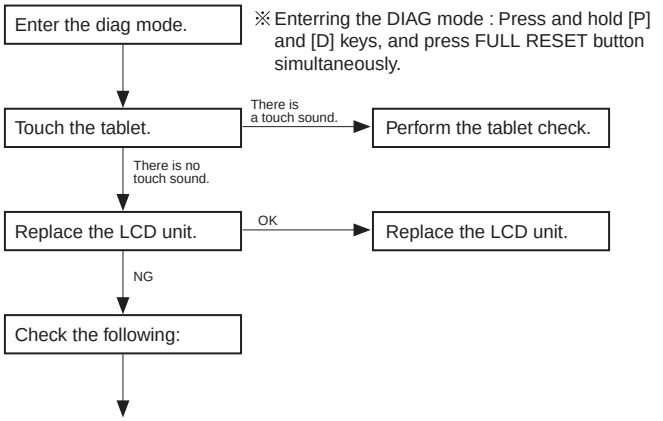
∗ Enter the diag mode and execute "NO10 FRONTLIGHT check.", and push Calendar key.

1) Check that the inverter unit is properly connected to the connector.

2) Is VCC to the inverter unit normal?
(Is F302 not blown off?) → VCC: 4.5V or above

3) Check the level of FLPWM.
→ FLPWM (TP305): Check that the level is not 0V. (Normally operates on 3.3V at about 170Hz.)

4. INPUT OPERATIONS WITH THE TABLET ARE INVALID

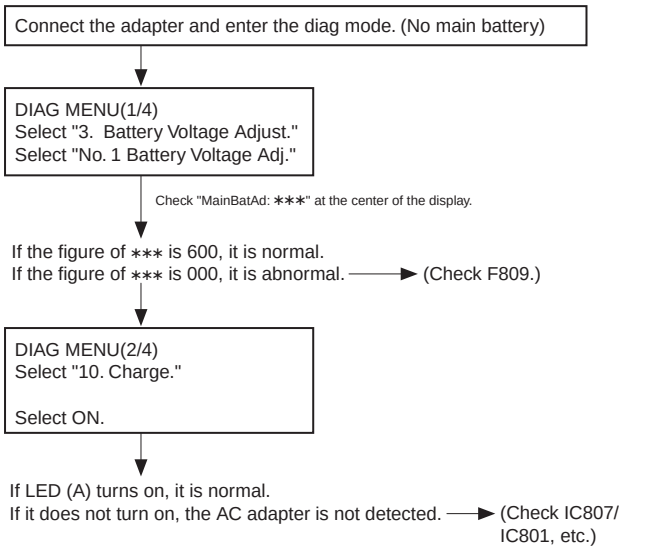

Enter the diag mode.
※ Enterring the DIAG mode : Press and hold [P] and [D] keys, and press FULL RESET button simultaneously.
Touch the tablet.
There is a touch sound.
Perform the tablet check.
There is no touch sound.
Replace the LCD unit.
OK
Replace the LCD unit.
NG
Check the following:

1) Are figures indicated on AIN0 and AIN1 on the lower side of the diag menu?
→ No display: Check soldering of IC501/IC901.

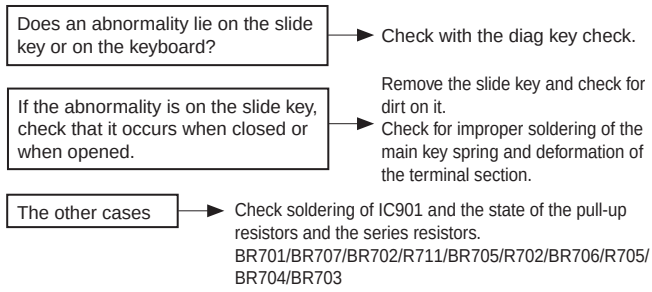
2) Does X903 oscillate? (X903 = 18.432 MHz)

3) Is FPC of the tablet disconnected? Is it properly connected to the connector?

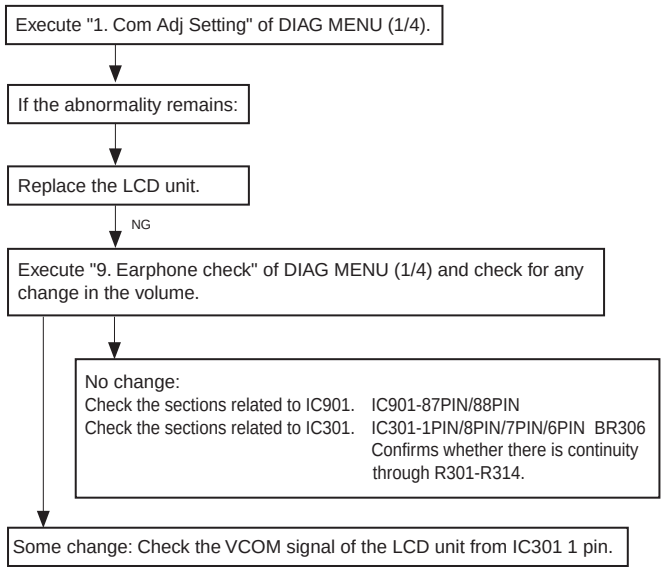
5. CANNOT BE DISCHARGED


Connect the adapter and enter the diag mode. (No main battery)
DIAG MENU(1/4)
Select "3. Battery Voltage Adjust."
Select "No. 1 Battery Voltage Adj."
Check "MainBatAd: ∗∗∗" at the center of the display.
If the figure of ∗∗∗ is 600, it is normal.
If the figure of ∗∗∗ is 000, it is abnormal. → (Check F809.)
DIAG MENU(2/4)
Select "10. Charge."
Select ON.
If LED (A) turns on, it is normal.
If it does not turn on, the AC adapter is not detected. → (Check IC807/ IC801, etc.)

6. KEY INPUTS ARE INVALID.


Does an abnormality lie on the slide key or on the keyboard?
Check with the diag key check.
If the abnormality is on the slide key, check that it occurs when closed or when opened.
Remove the slide key and check for dirt on it.
Check for improper soldering of the main key spring and deformation of the terminal section.
The other cases
Check soldering of IC901 and the state of the pull-up resistors and the series resistors.
BR701/BR707/BR702/R711/BR705/R702/BR706/R705/ BR704/BR703

7. ABNORMAL DISPLAY COLORS


Execute "1. Com Adj Setting" of DIAG MENU (1/4).
If the abnormality remains:
Replace the LCD unit.
NG
Execute "9. Earphone check" of DIAG MENU (1/4) and check for any change in the volume.
No change:
Check the sections related to IC901. IC901-87PIN/88PIN
Check the sections related to IC301. IC301-1PIN/8PIN/7PIN/6PIN BR306
Confirms whether there is continuity through R301-R314.
Some change: Check the VCOM signal of the LCD unit from IC301 1 pin.

8. SHORT BATTERY LIFE

First of all, explain that the battery life varies depending on the use environment and the operating conditions.

1) According to “BATTERY VOLTAGE ADJUSTMENT PROCEDURE” on the Service Manual, check the set values. (If necessary, make setting again.
2) Execute “CURRENT COMSUMPTION CHECK” on the Service Manual to check the current value.
3) Replace the battery pack.

9. THE CF CARD (SD CARD) IS NOT RECOGNIZED. / WHEN THE CF CARD IS INSERTED, NO OPERATION IS PERFORMED

First of all, check for deformation of the connector terminal of each card.

1) Check CF CD and SD CD on the right lower side of the diag menu. → All should be "H."

2) Insert the CF card and the SD card, and check again.

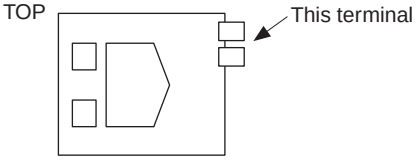
↓

All should be "L."

↓ NG(Remains at "H")

The card is not recognized.

- When the CF card is not recognized : Check "CD" pin of the connector and check CCD∗∗ of BR403 and IC401.
- When the SD card is not recognized : Check soldering of the terminals outside of the connector of CN1002 of the sub PWB.
  Check IC901 and BR906.

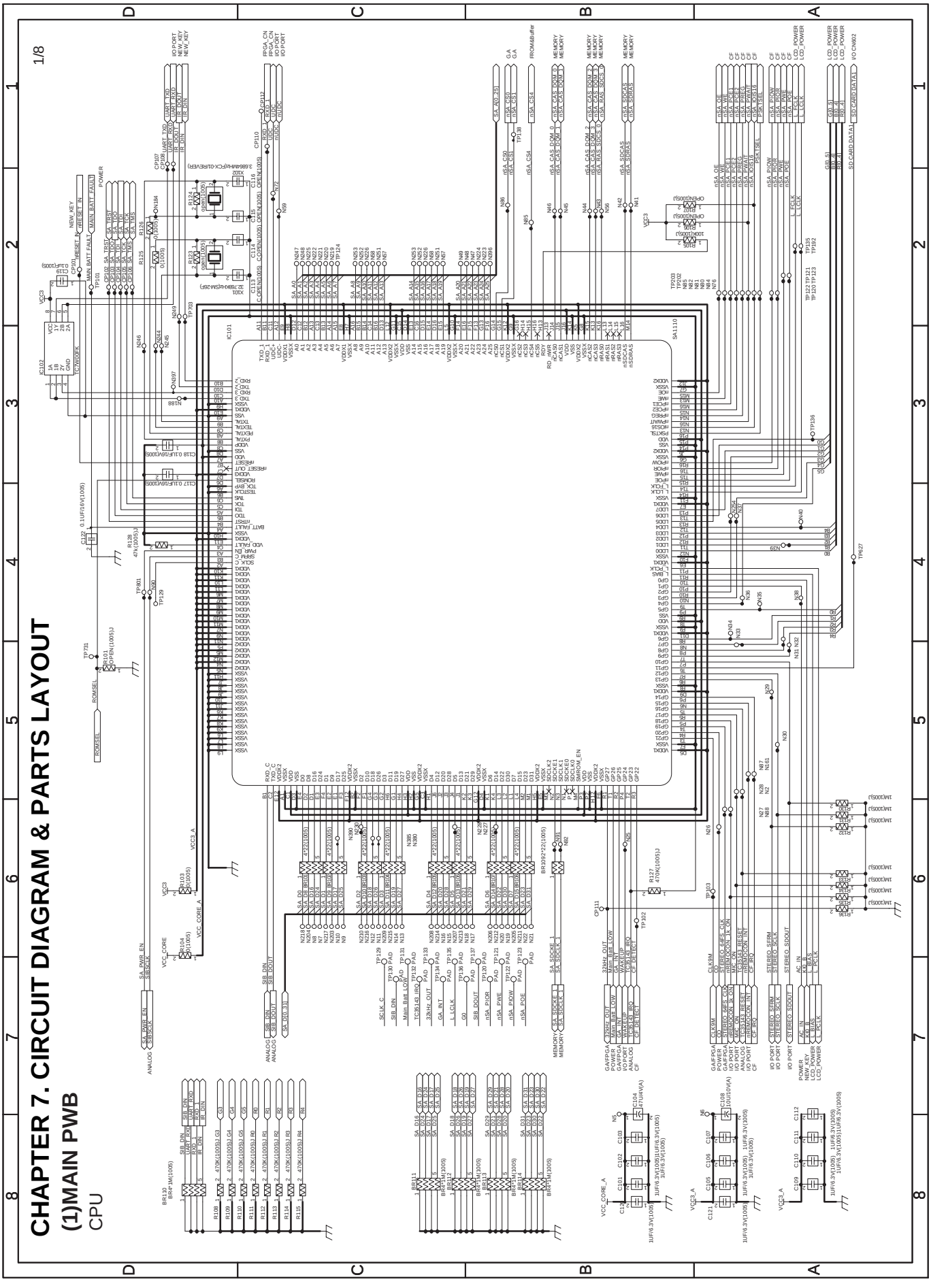


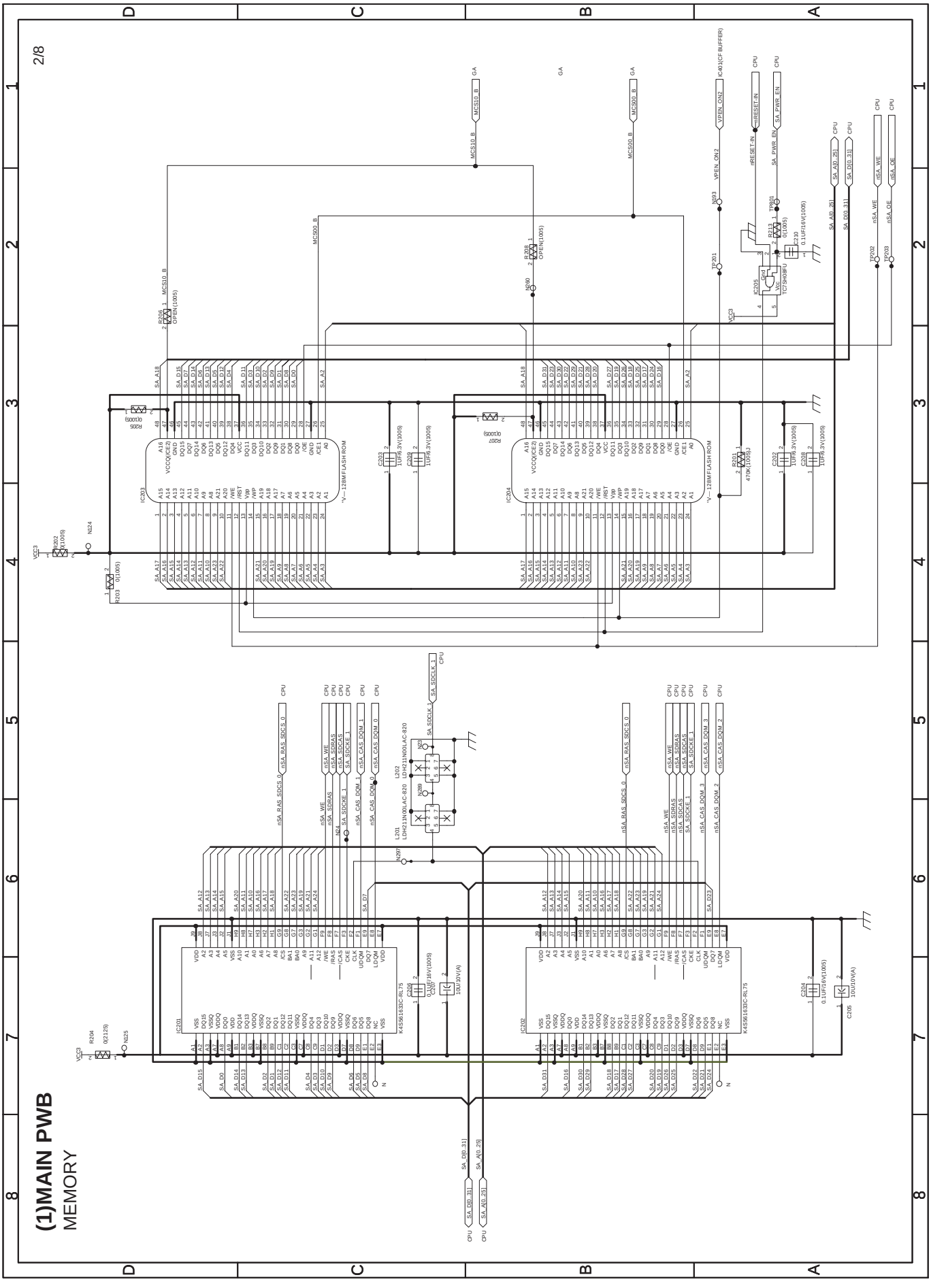
3) When the CF card is inserted, no operation is performed. → Check with the OS.
When the "WAIT" signal of the card is at "LOW", no operation is performed. (Wait is applied to the operation.)
Check IC401 and BR402.
(Check that soldering is properly made and that the resistors are not broken.)

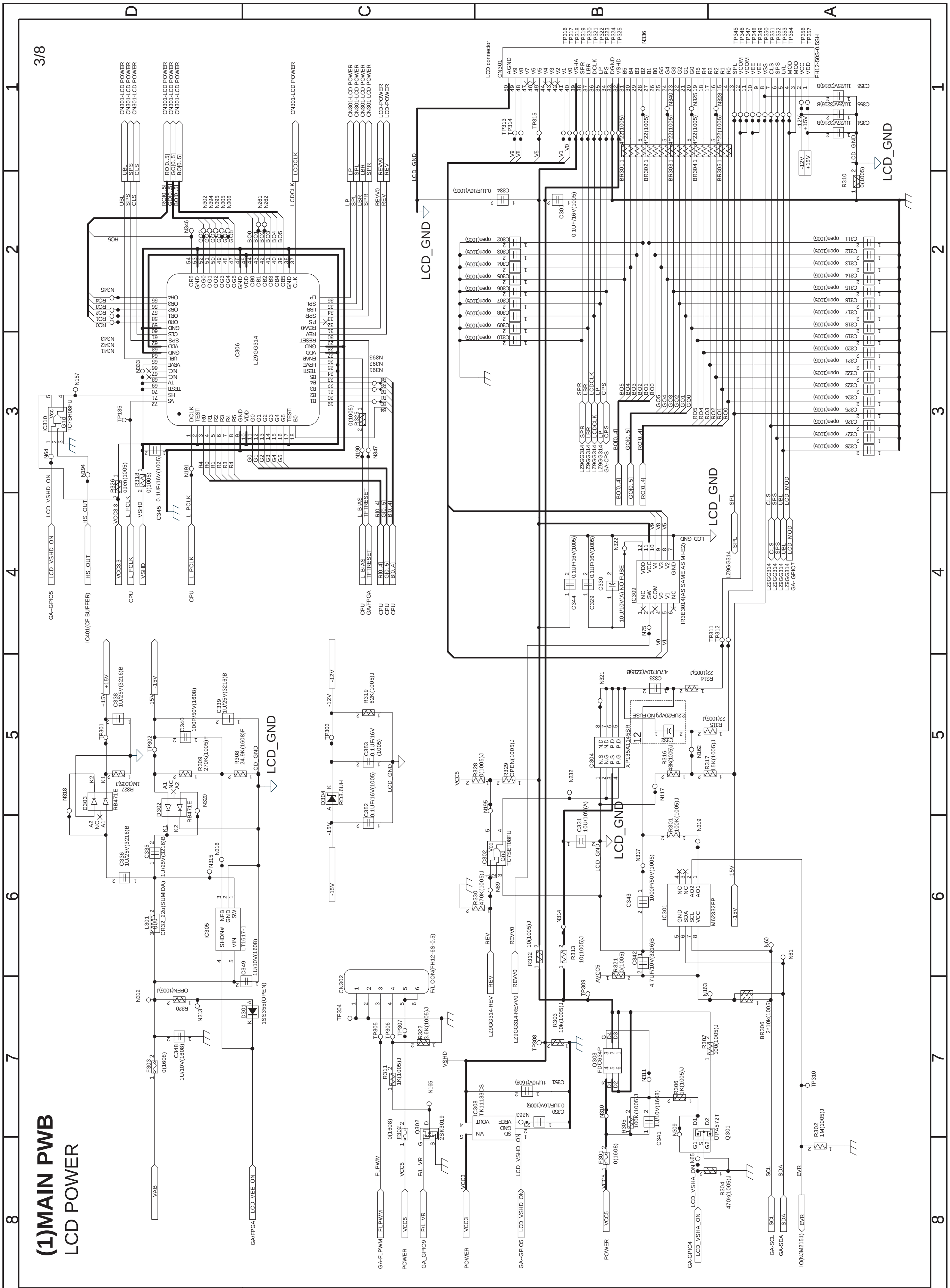
CHAPTER 7. CIRCUIT DIAGRAM & PARTS LAYOUT

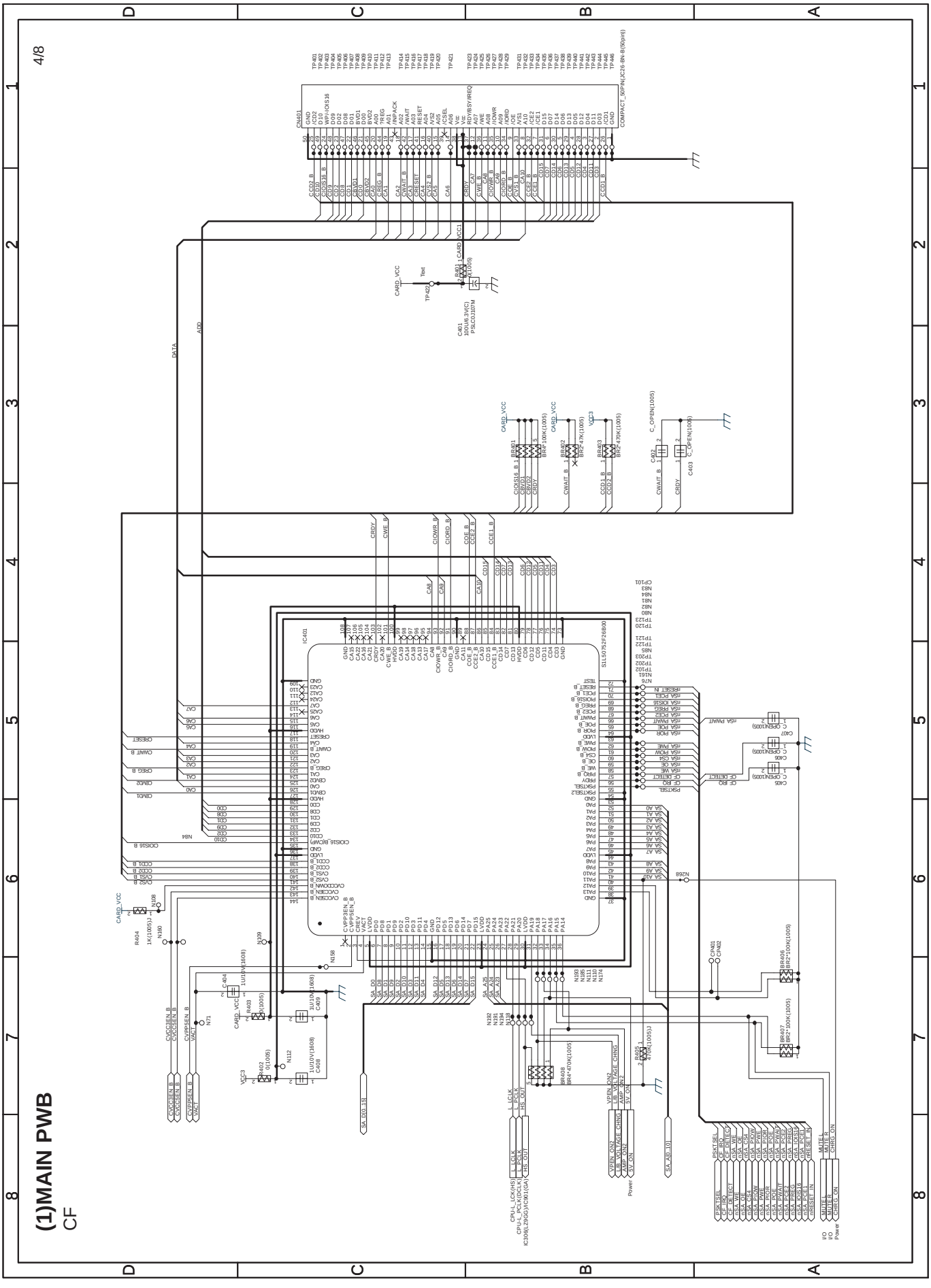
(1)MAIN PWB

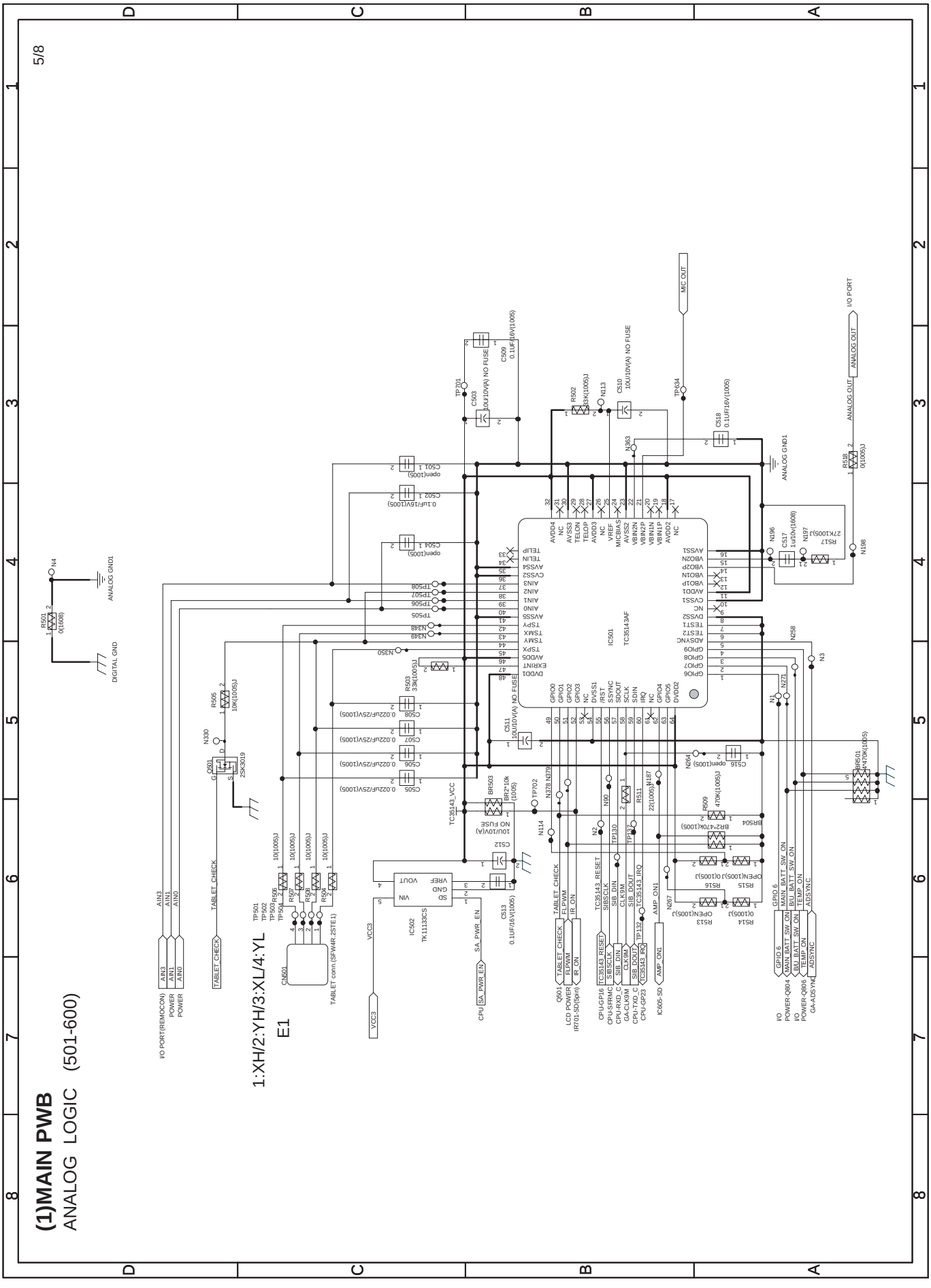
CPU

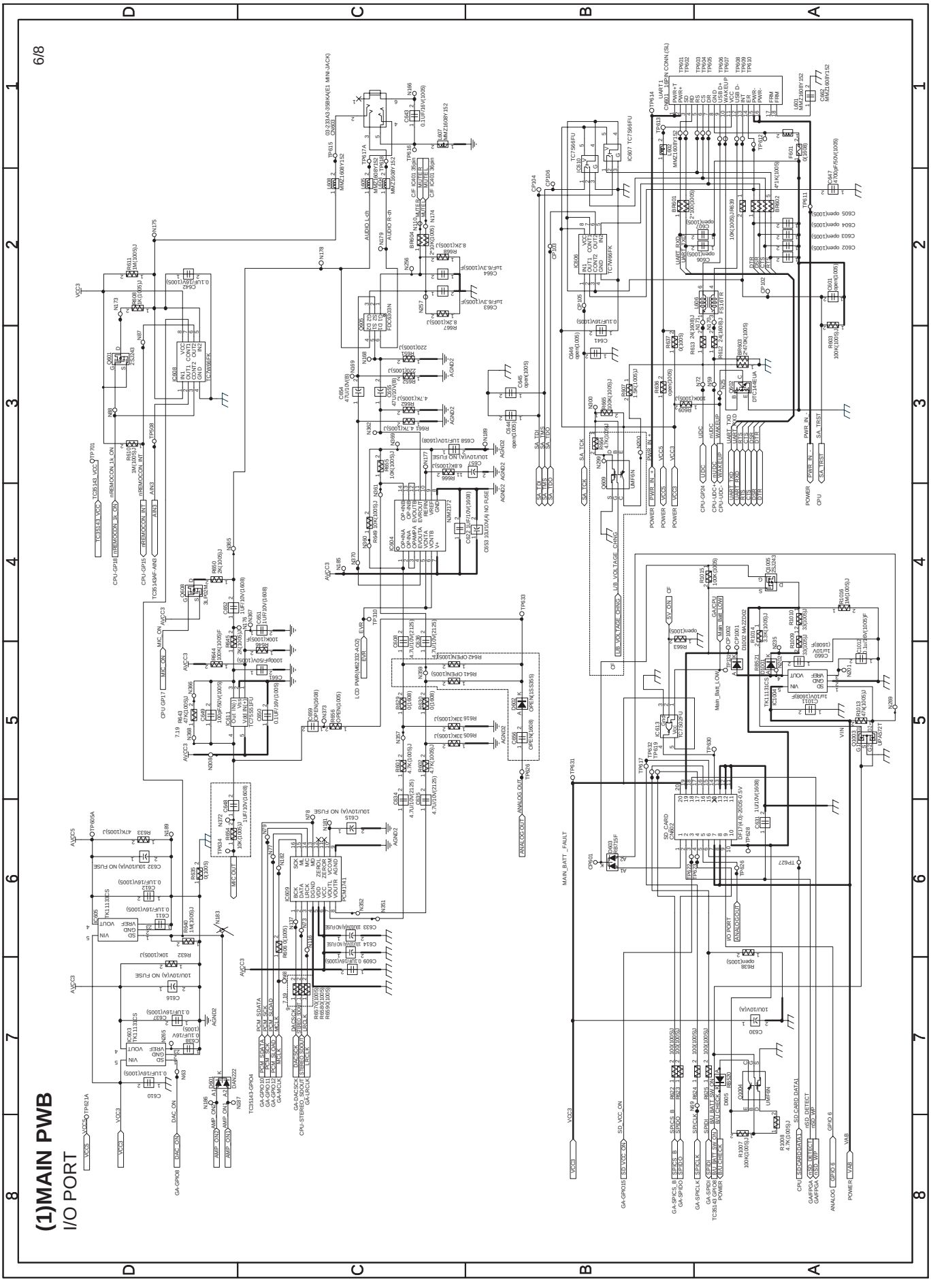


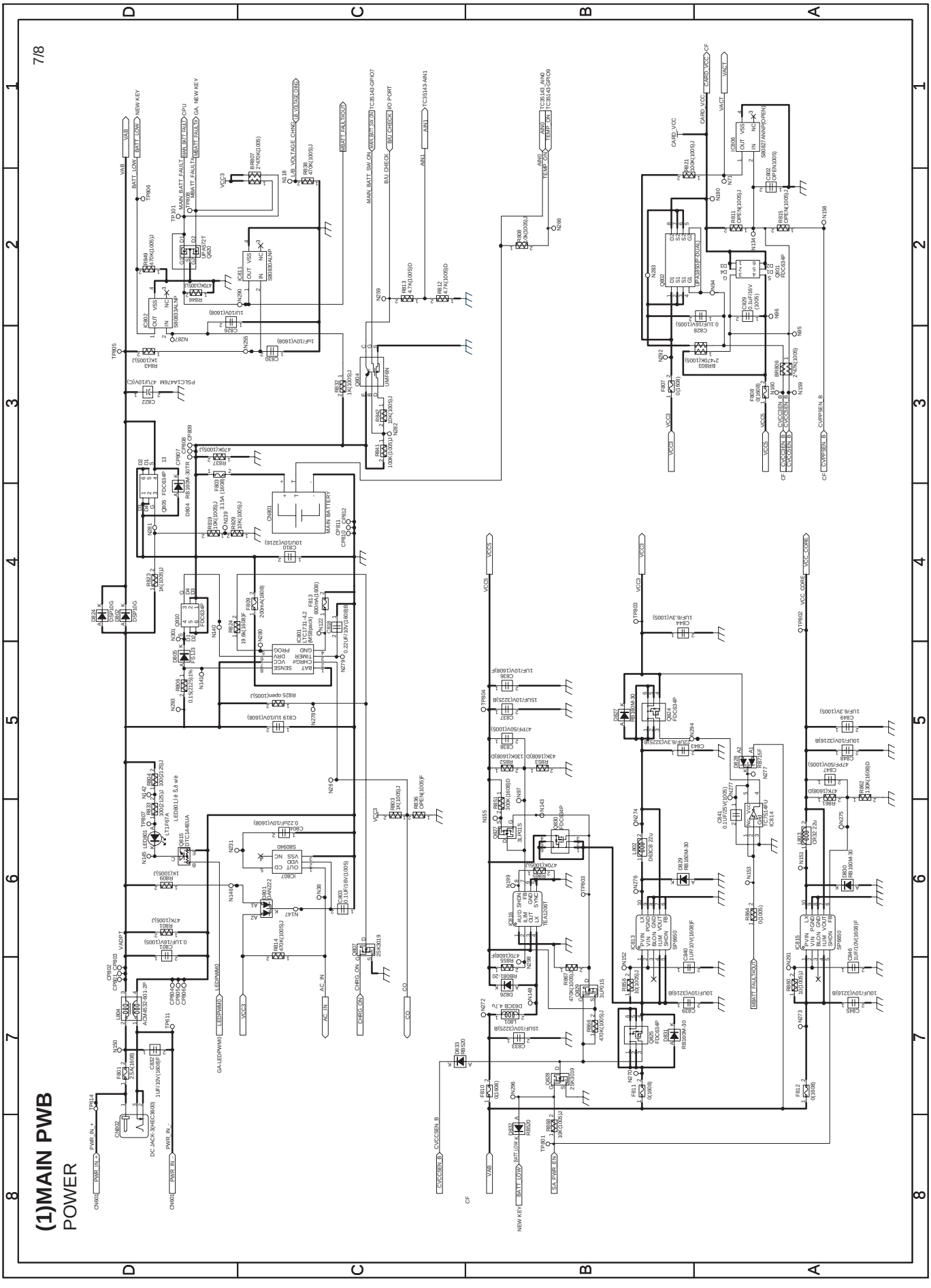

(1)MAIN PWB
MEMORY
2/8

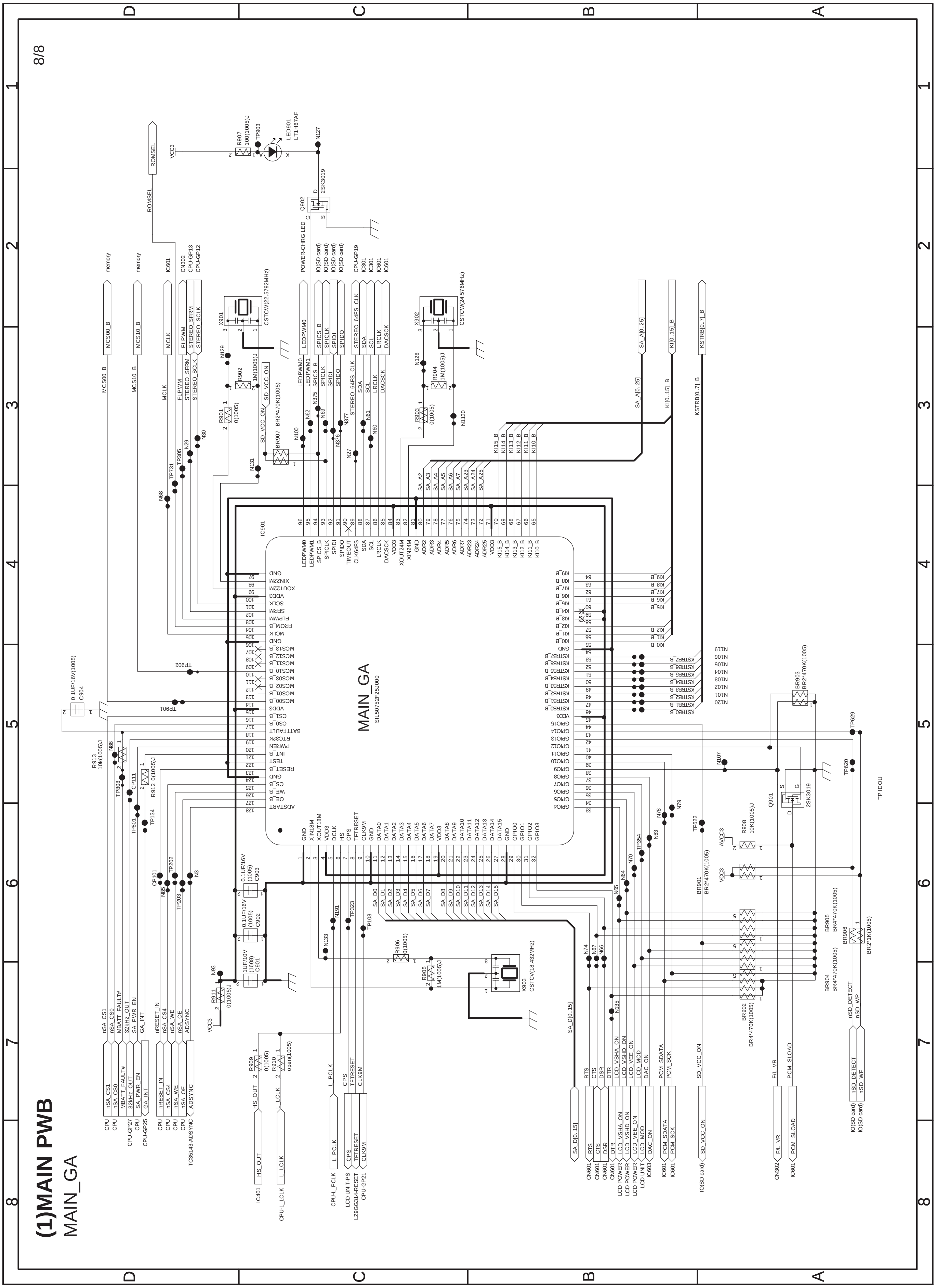

(1)MAIN PWB
LCD POWER
3/8

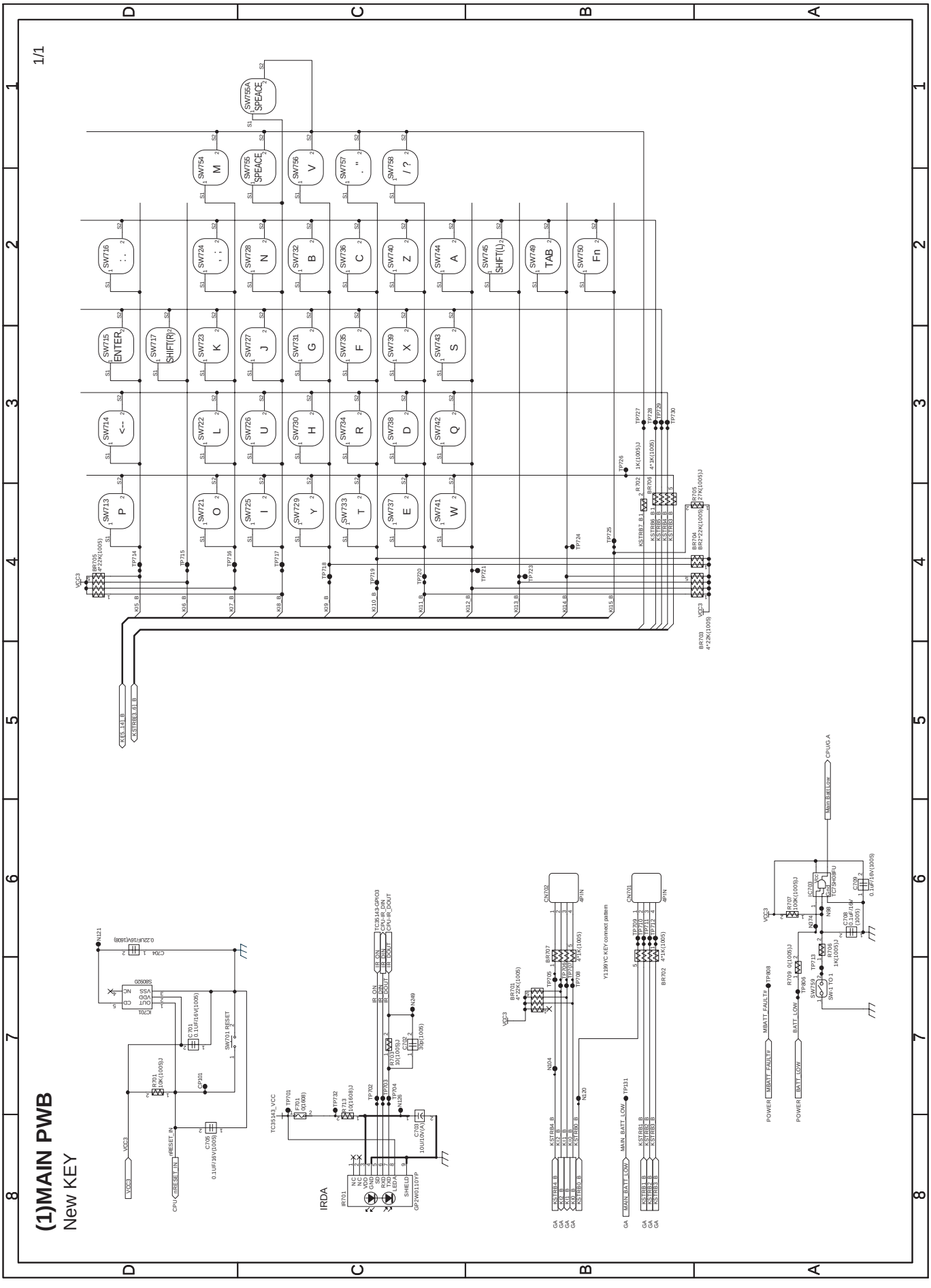

4/8
(1)MAIN PWB
CF

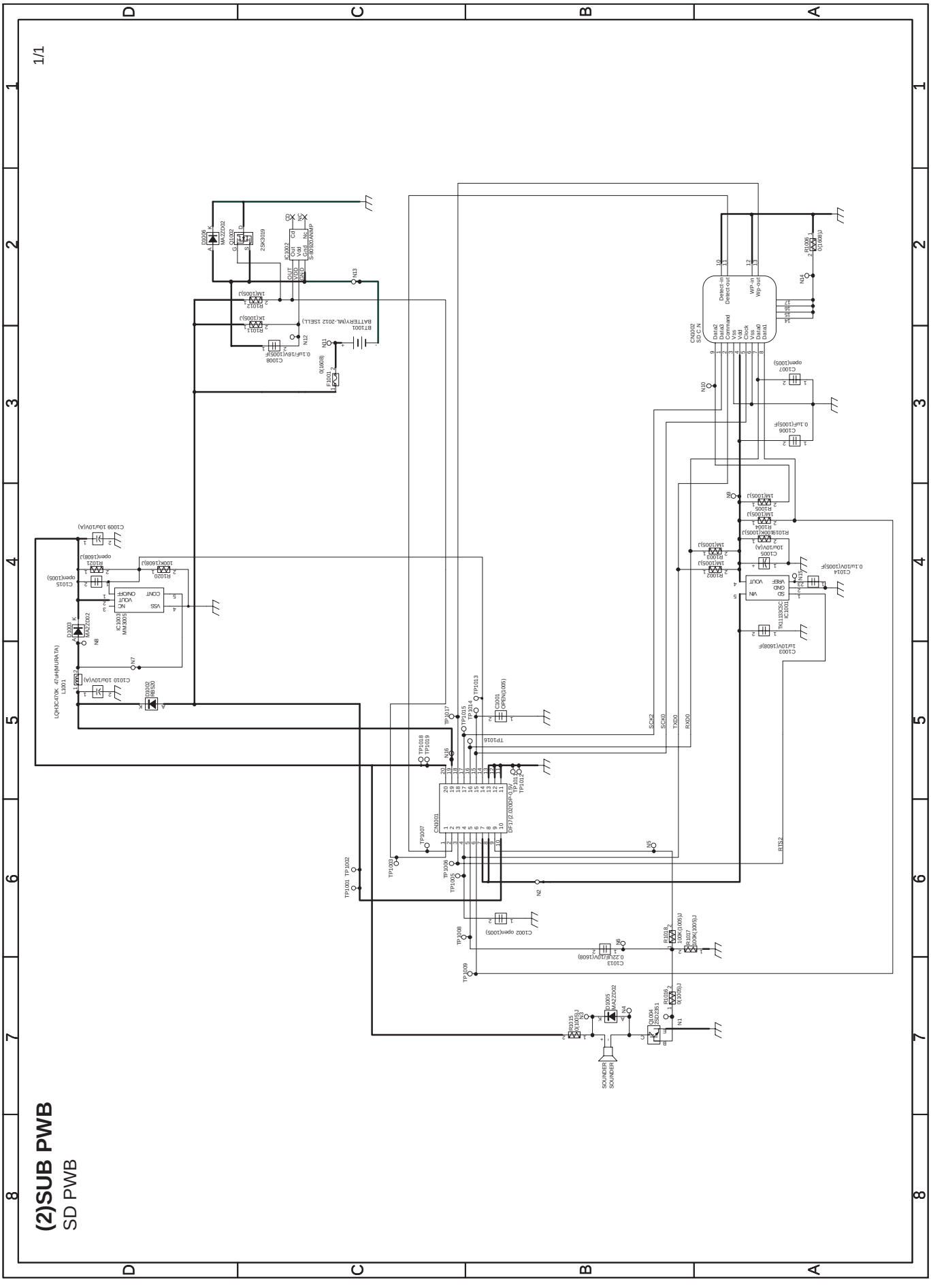

(1)MAIN PWB
ANALOG LOGIC (501-600)
5/8
1:XH/2:YH/3:XL/4:YL
E1
IC501
TC35143AF
IC502
TK11133CS
CN601
TABLET conn.(SFW4R-2STE1)
I/O PORT(REMOCON)
TABLET_CHECK
ANALOG GND1
DIGITAL GND
MIC OUT
ANALOG OUT
I/O PORT
VCC3
SA_PWR_EN
AMP_ON1
ADSYNC
TEMP_ON
MAIN_BATT_SW_ON
BU_BATT_SW_ON


6/8
(1)MAIN PWB
I/O PORT


7/8
(1)MAIN PWB
POWER


(1)MAIN PWB
MAIN_GA
8/8
IC901
MAIN_GA
SIL50752F25J000
X901 CSTCW(22.5792MHz)
X902 CSTCW(24.576MHz)
X903 CSTCV(18.432MHz)
LED901 LT1H67AF
Q902 2SK3019
Q901 2SK3019
ROMSEL
MCS00_B memory
MCS10_B memory
MCLK IC601
FLPWM CN302
STEREO_SFRM CPU-GP13
STEREO_SCLK CPU-GP12
LEDPWM0 POWER-CHRG LED
SPICS_B IO(SD card)
SPICLK IO(SD card)
SPIDI IO(SD card)
SPIDO IO(SD card)
STEREO_64FS_CLK CPU-GP19
SDA IC301
SCL IC301
LRCLK IC601
DACSCK IC601
SA_A[0..25]
KI[0..15]_B
KSTRB[0..7]_B
CPU nSA_CS1
CPU nSA_CS0
CPU-GP27 MBATT_FAULT#
CPU 32kHz_OUT
CPU-GP25 SA_PWR_EN
GA_INT
CPU nRESET_IN
CPU nSA_CS4
CPU nSA_WE
CPU nSA_OE
TC35143-ADSYNC ADSYNC
IC401 HS_OUT
CPU-L_LCLK L_LCLK
CPU-L_PCLK L_PCLK
LCD UNIT-PS CPS
LZ9GG314-RESET TFTRESET
CPU-GP21 CLK9M
SA_D[0..15]
CN601 RTS
CN601 CTS
CN601 DSR
CN601 DTR
LCD POWER LCD_VSHA_ON
LCD POWER LCD_VSHD_ON
LCD POWER LCD_VEE_ON
LCD UNIT LCD_MOD
IC603 DAC_ON
IC601 PCM_SDATA
IC601 PCM_SCK
IO(SD card) SD_VCC_ON
CN302 F/L_VR
IC601 PCM_SLOAD
IO(SD card) nSD_DETECT
IO(SD card) nSD_WP

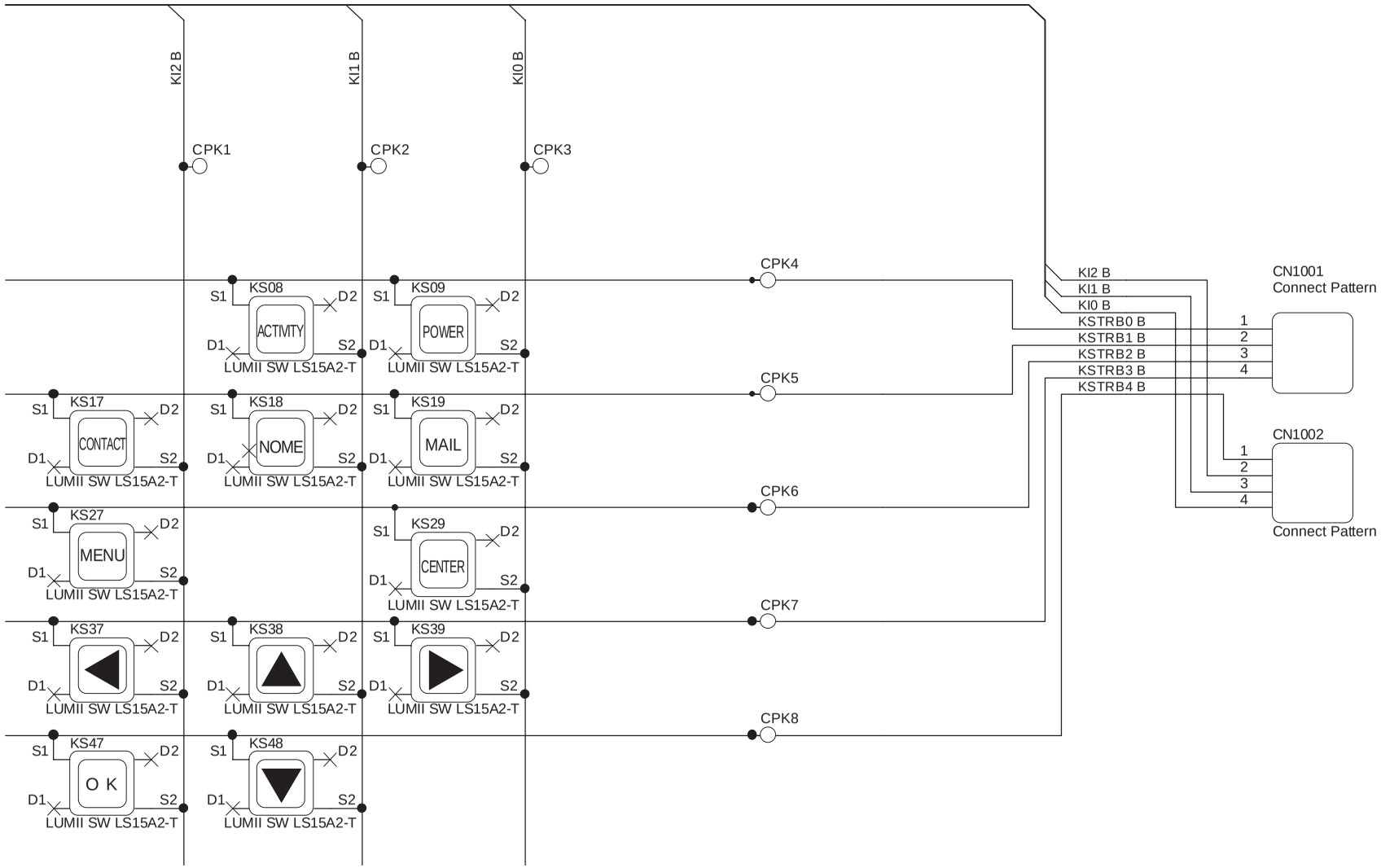

(1)MAIN PWB
New KEY
1/1
SW716 : .
SW724 ; ;
SW728 N
SW732 B
SW736 C
SW740 Z
SW744 A
SW745 SHIFT(L)
SW749 TAB
SW750 Fn
SW754 M
SW755 SPEACE
SW756 V
SW757 , "
SW758 / ?
SW755A SPEACE
SW715 ENTER
SW717 SHIFT(R)
SW723 K
SW727 J
SW731 G
SW735 F
SW739 X
SW743 S
SW714 <--
SW722 L
SW726 U
SW730 H
SW734 R
SW738 D
SW742 Q
SW713 P
SW721 O
SW725 I
SW729 Y
SW733 T
SW737 E
SW741 W
BR705 4*22K(1005)
BR703 4*22K(1005)
BR704 4*22K(1005)
BR702 4*1K(1005)
KSTRB7_B
KSTRB6_B
KSTRB5_B
KSTRB4_B
KSTRB3_B
KSTRB2_B
KSTRB1_B
KSTRB0_B
K15_7-I1_B
KSTRB3_6-I1_B
IRDA
IR701
GP2W0110YP
TC35143_VCC
TC35143-GPIO3
CPU-IR_DIN
CPU-IR_DOUT
IR_ON
IR_DIN
IR_DOUT
R703 10(1005)J
C707 330P(1005)
C720 10U/10V(A)
SW701 RESET
C701 0.1UF/16V(1005)
IC701 S80920
R701 10K(1005)J
CP101
C705 0.1UF/16V(1005)
C704 0.22UF/25V(1608)
VCC3
nRESET_IN
CPU nRESET_IN
CN702
CN701
4PIN
Y1:199°C KEY correct pattern
MAIN_BATT_LOW
POWER MBATT_FAULT
POWER BATT_LOW
Main Batt Low
CPUG.A
R709 0(1005)J
R706 1K(1005)J
SW759 SW-734
C709 0.1UF/16V(1005)
C708 0.1UF/16V(1005)
C710 470P(1005)
R707 470K(1005)J


(2)SUB PWB
SD PWB
1/1

(3)KEY PWB

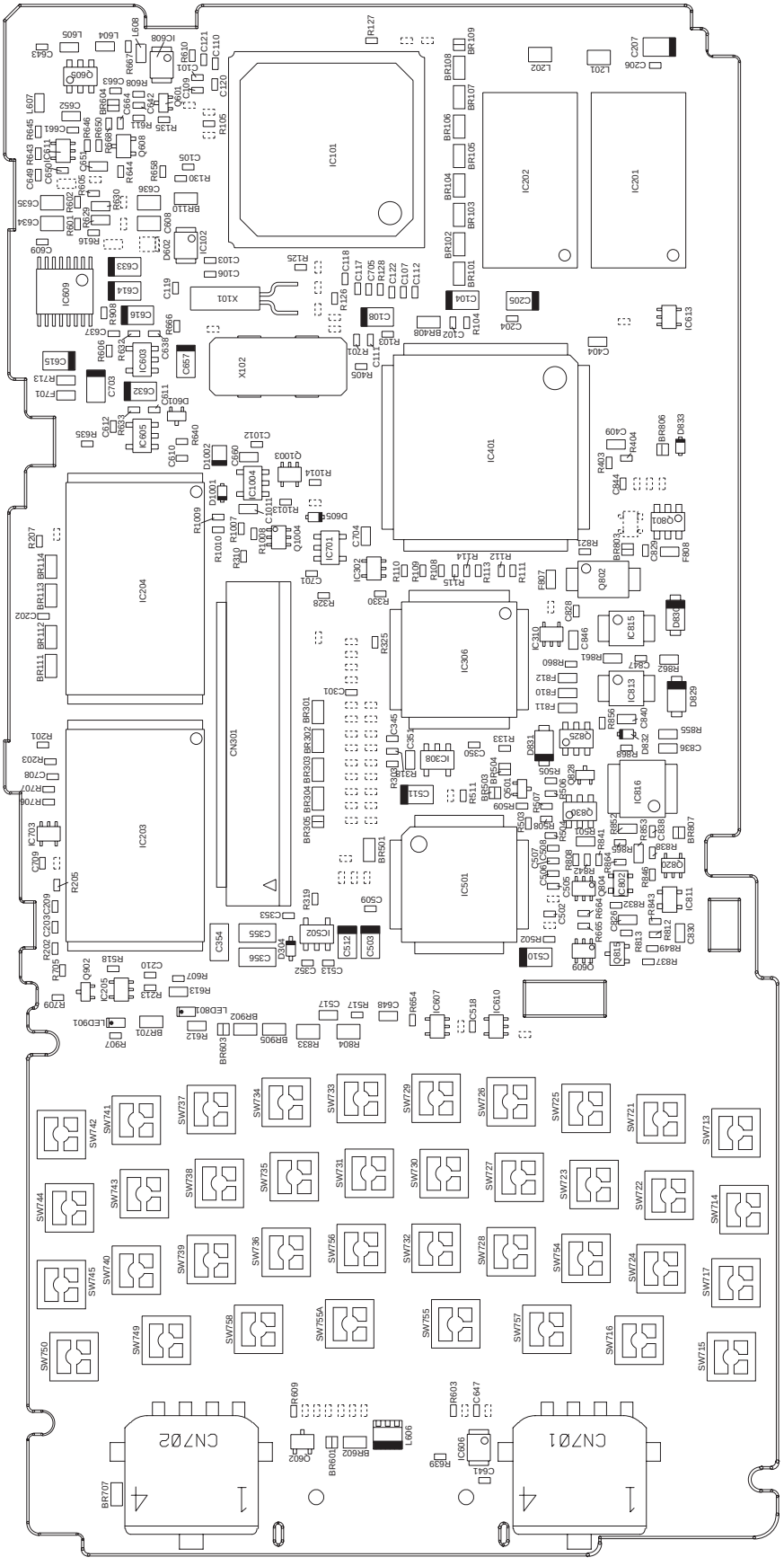
SLIDE KEY

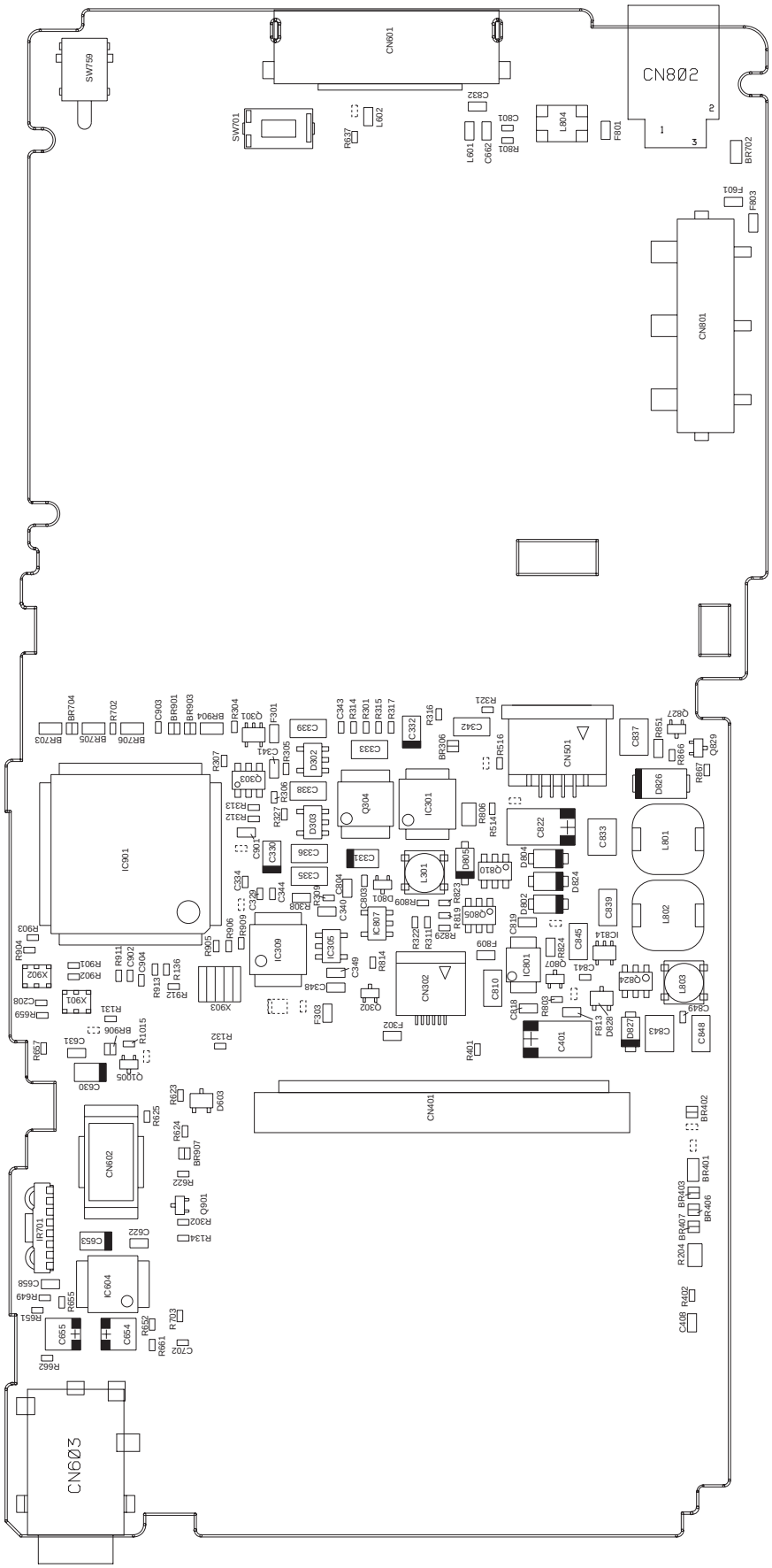
1/1



PARTS LAYOUT

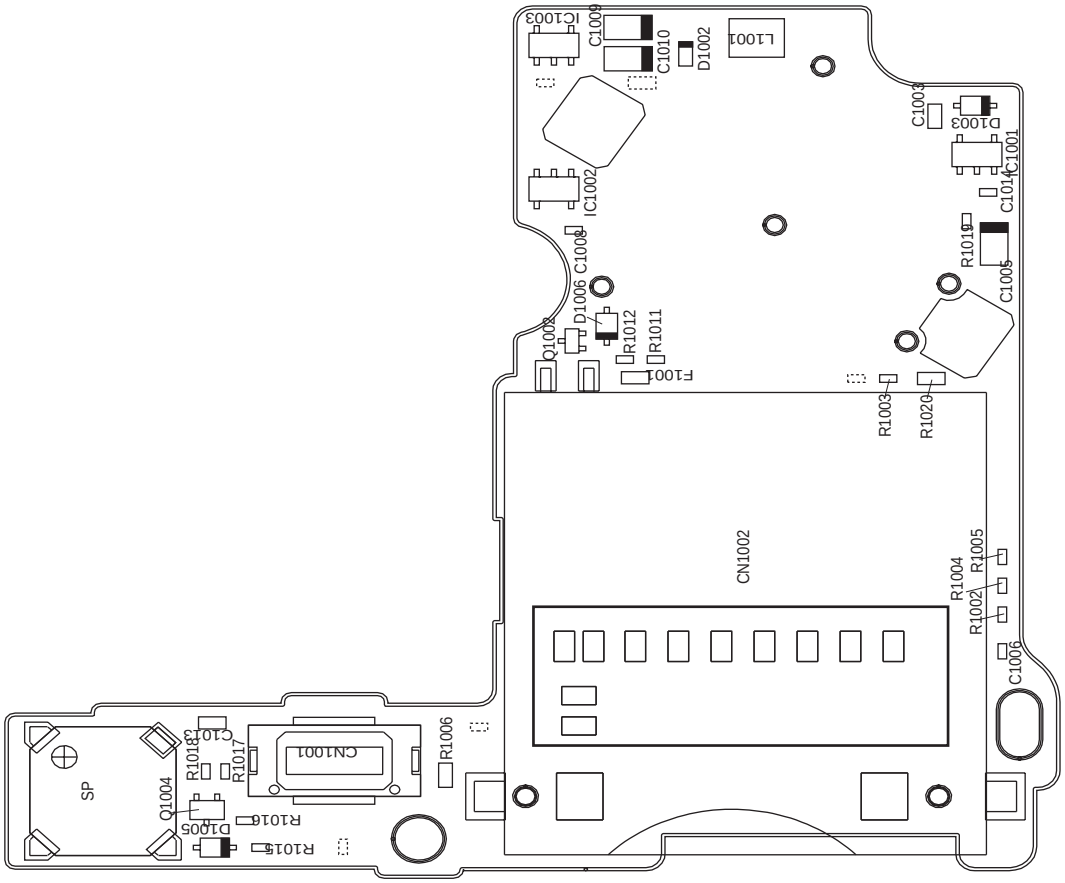
Main PWB, Side A



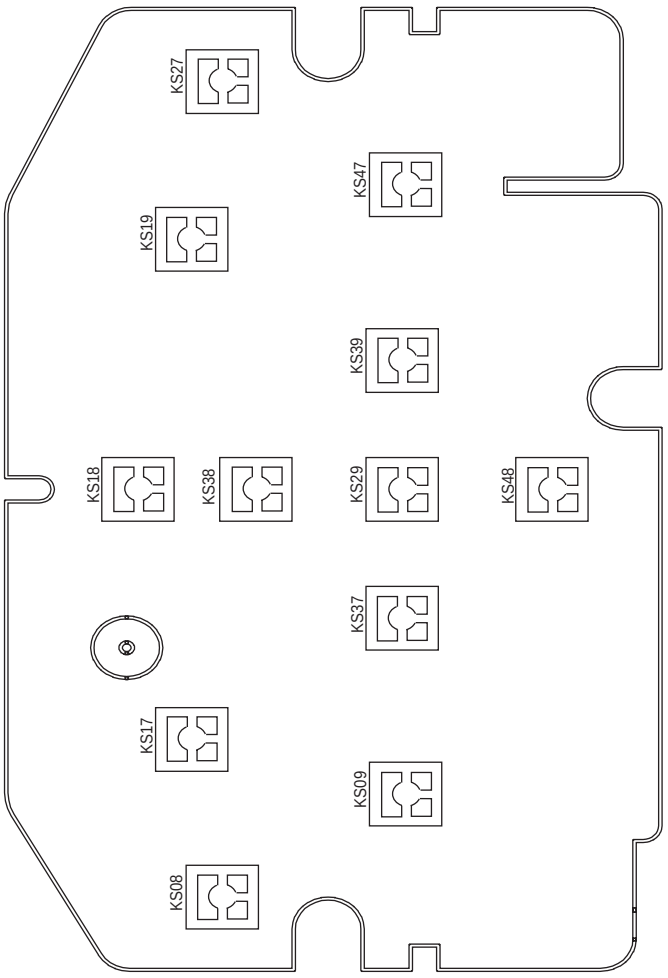


Main PWB, Side B

Sub PWB



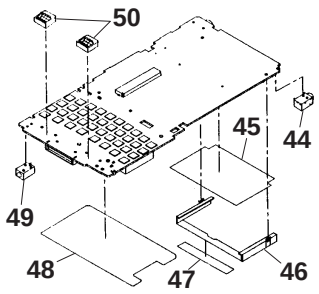
Key PWB



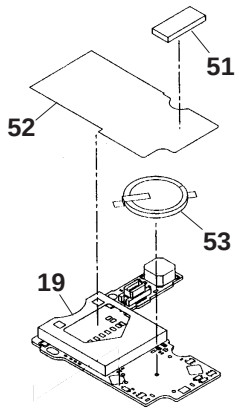
■ Parts guide

1 Exteriors

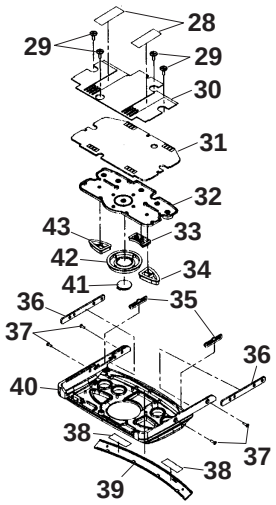
MAIN PWB UNIT



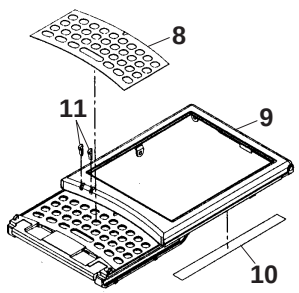
SUB PWB UNIT



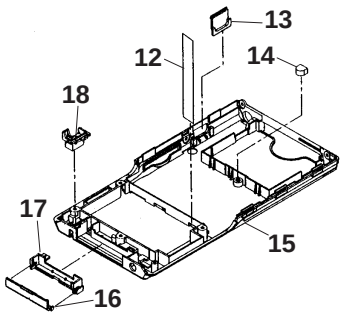
SLIDE COVER UNIT



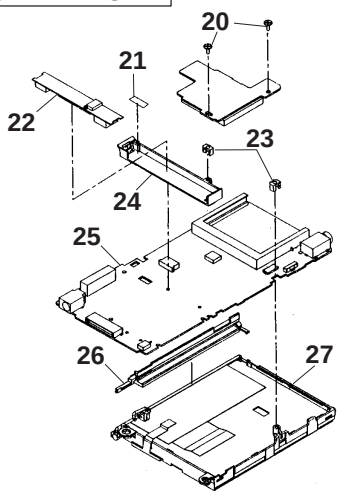
UPPER CABINET UNIT

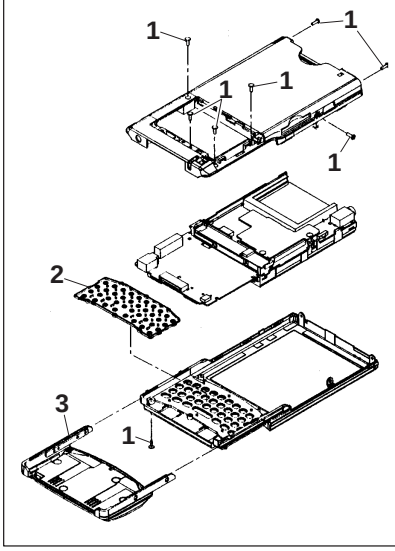


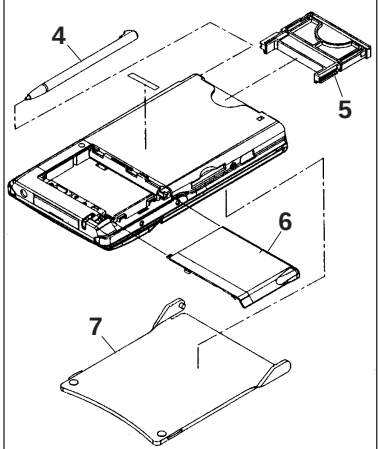
LOWER CABINET UNIT



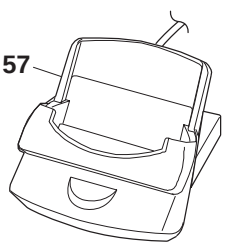
LCD+PWB UNIT







DOCKING STATION



CCP00163

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LX−BZ1026YCZZ	AA		C	Screw C (M14)
2	PGUMM1031YCZ1	AP		C	Key rubber A
3	DUNTG2197YCS2	BC	N	E	Slide cover unit
4	CPENP1008YC01	AQ		C	Stylus
5	GiTA−1006YCB1	AD		D	CF slot protection card
6	GFTAB1068YCZZ	AG		D	Battery comparment lid
7	CCŌVH1032YC02	AP		D	Display protection cover [SEC/SECL]
	CCŌVH1032YC01	AN		D	Display protection cover [OTHER,SUK,SCA/SCNZ,SEEG,SRH]
8	PSHEZ1100YCZ1	AG		C	Key panel [SEC/SECL]
	PSHEZ1100YCZ4		N	D	Key panel [OTHER,SUK,SCA/SCNZ,SEEG,SRH]
9	GCABB1128YCZZ	AT		D	Upper cabinet
10	PSLDP1088YCZZ	AD		C	Tablet upper mask
11	PFiLW1036YCZZ	AC		D	LED inductor
12	PTPEC1101YCZZ	AC		D	Battery take-out ribbon
13	PFiLW1035YCZZ	AC		D	IR filter
14	PCUSS1081YCZZ	AB		C	Nut cushion
15	GCABA1132YCZ2	AR	N	D	Lower cabinet
16	GFTAA1069YCZZ	AD		D	I/O cover
17	LHLDZ1057YCZZ	AC		C	I/O holder
18	JKNBZ1096YCZZ	AC		C	Battery replacement switch
19	DUNTK2249YCS1	BA	N	E	Sub PWB unit [not include No.51,52,53]
20	LX−BZ1193CCZZ	AA		C	Screw D (M1.7)
21	PTPEH1103YCZZ	AA		D	Invertor fixing tape
22	RUNTZ1018YCZZ	BA		E	Invertor unit
23	PCAP−1008YCZZ	AC		C	Boss cap
24	LHLDZ1064YCZZ	AD		C	Invertor holder
25	DUNTK2247YCZZ	CE	N	E	Main PWB unit [include No.44~50]
26	LHLDZ1062YCZZ	AD		C	Stylus holder
27	DUNTL2262YCZZ	CA		E	LCD unit
28	PTPEH1102YCZZ	AC		D	Slideing sheet A
29	LX−BZ1239CC01	AB		C	Screw B
30	PSHEZ1101YCZZ	AH		C	Key PWB sliding sheet
31	DUNTK2249YCS2	AR	N	E	Key PWB unit
32	PGUMM1030YCZ1	AL		C	Key rubber B
33	JKNBZ1099YCZ1	AG		C	Key top A3 (HOME)
34	JKNBZ1093YCZ1	AG		C	Key top A1 (Cancel)
35	MLŌK−1026YCZZ	AC		C	Slide cover lock
36	LANGK1031YCZZ	AF		C	Slide cover fixture
37	LX−BZ1048YC01	AB		C	Screw A
38	PTPEH1104YCZZ	AA		C	Slide cover panel fixing tape
39	HPNL−1004YCZZ	AH		D	Slide cover panel
40	GCABB1129YCZ1	AR		D	Slide cover cabinet
41	JKNBZ1097YCZZ	AF		C	Key top C
42	JKNBZ1095YCZZ	AG		C	Key top B
43	JKNBZ1094YCZ1	AG		C	Key top A2 (OK)
44	QJAKC1015YCZZ	AF		C	Stereo headphone jack [CN603]
45	PZETL1074YCZZ	AD		C	PWB insulation sheet
46	KMEC−1013YCZZ	AN		D	CF card connector frame [CN401]
47	PTPEH1108YCZZ	AB		D	CF tape
48	PZETL1079YCZZ	AD		C	Battery section insulation sheet
49	QCNCW1339AC0C	AG		C	AC adapter jack (3pin)(HEC3600-010010) [CN802]
50	QTANB1051YCZZ	AR		C	Contact spring unit [CN701,CN702]
51	PCUSS1080YCZZ	AC		C	Back up battery cushion
52	PZETL1085YCZZ	AD		D	Back up battery insulate sheet
53	RDNTL0001YCZZ	AM		B	Litume battery (ML2016TT2)
57	RUNT−1020YCA1	BK	N	E	Docking station

2 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
⚠ 1	QACCD1311QCZZ	AN		B	AC cord (10A-BUSH2M)	[SEC/SECL,OTHER]
⚠ 1	QACCB3321QCZZ	BA		B	AC cord (13A-BUSH2M)	[SUK,SRH]
⚠ 1	QACCE3321QCZZ	AQ		B	AC cord (2.5A-BUSH2M)	[SEEG]
⚠ 1	QACCL3321QCZZ	AR		B	AC cord (7.5A BUSH2M)	[SCA/SCNZ]
⚠ 2	RADPA1017YCZZ	BB	N	B	AC adaptor	
3	PSHEZ1108YCZZ	AD		C	Support sticker(for card ejection)	
4	TiNSE1273YCZZ	AH	N	D	Start up guide	
5	TGANE1003QCZ1	AF		D	Warranty card(EU)	[SUK,SEEG]
5	TGANE1114CCN1	AB		D	Warranty card	[SCA/SCNZ]
6	TiNSE1272YCZZ	AL	N	D	Operation manual	
7	TiNSE1274YCZZ	AG	N	D	USB Driver install manual	
9	SPAKC1664YCZZ	AG	N	D	Packing case	
10	SPAK-546ECCZZ	AB		D	Vinyl bag (125×230)	[for SET]
11	SPAKA1675YCZZ	AD	N	D	Set add	
12	SPAKA1676YCZZ	AF	N	D	Accessory add	
13	TCADZ1446YCZZ	AD	N	D	Wireless connection card information	[SEC/SECL]
14	SSAKA5004CCZZ	AA		D	Vinyl bag	[for AC cord]
15	SSAKH0011HCZZ	AA		D	Vinyl bag (60×140)	[for Support sticker]
16	TLABZ1286YCZZ	AC	N	D	Wireless connection information label	[SEC/SECL]
17	TCADZ1431YCZZ	AC		D	EULA card	
19	TLABS1284YCZZ		N	D	EAN code label	[OTHER,SUK,SCA/SCNZ,SEEG,SRH]
21	CDSKA1037YC01	AL	N	D	CD-ROM	

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	QCNCW1016YC50	AH		C	Connector (50pin)	[CN301]
2	QCNCW1033YC04	AE		C	Connector (4pin)	[CN501]
3	QCNCW1046YC16	AL		C	Connector (Main-Sub)(16pin I/O)	[CN601]
4	QCNCW1054YC06	AF		C	Connector (6pin)(FH12-6S-0.5SH)	[CN302]
5	QCNCW1088YC50	AN		C	Connector (50pin)	[CN401]
6	QCNCW1112YC20	AH		C	Connector (DF17(4.0)-20DS-0.5V)	[CN602]
⚠ 7	QFS-L1036YCZZ	AD		A	Fuse (KAB 2.5A)	[F801]
⚠ 8	QFS-L1038YCZZ	AD		A	Fuse (KAB 3.15A)	[F803]
⚠ 9	QFS-L2016XHZZ	AD		A	Fuse (KAB 200mA)	[F809]
⚠ 10	QFS-L631AAFNZ	AD		A	Fuse (2A)	[F813]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW713,SW714,SW715,SW716,SW717]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW721,SW722,SW723,SW724,SW725]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW726,SW727,SW728,SW729,SW730]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW731,SW732,SW733,SW734,SW735]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW736,SW737,SW738,SW739,SW740]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW741,SW742,SW743,SW744,SW745]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW749,SW750,SW754,SW755,SW755A]
11	QSW-K0237AFZZ	AC		B	Tact switch	[SW756,SW757,SW758]
12	QSW-P1012PCZZ	AE		B	Push switch (SPVC21)(4p)	[SW759]
13	QSW-P1063YCZZ	AD		B	Reset sw	[SW701]
14	QTANB1054YCZZ	AL		C	Battery terminal unit cd	[CN801]
15	RCiLZ1051ACZZ	AC		C	Coil (MMZ1608Y152B)	[L604,L605,L607,L608,L601,L602 C662]
16	RCiLZ1112YCZZ	AF		C	Coil (CR32-22µH)	[L301,L803]
17	RCiLZ1118YCZZ	AF		C	Coil (D63CB 22µH)	[L802]
18	RCiLZ1119YCZZ	AF		C	Coil (D63CB_4.7µH)	[L801]
19	RCiLZ1123YCZZ	AM	N	C	Coil (LDH211N00LAC-820)	[L201,L202]
20	RC-KZ1002YCZZ	AF	N	C	Capacitor (C3225JB0J226MT)	[C843]
21	RC-KZ1003YCZZ	AF	N	C	Capacitor (C3225JB1A156MT)	[C833,C837]
22	RC-KZ1004YCZZ	AD	N	C	Capacitor (C3216JB1A106MT)	[C839,C845,C848]
23	RC-KZ2241RC1A	AB		C	Capacitor (10WV 0.22µF)	[C704,C804]
24	RC-KZ4752RC1A	AE		C	Capacitor (10WV 4.7µF)	[C333,C342]
25	RCŌRF1001YCZZ	AH		C	Core (ACM4532-601)	[L804]
26	RCRMC1023YCZZ	AE		B	Crystal (CSTCW2257MX03)	[X901]
27	RCRMC1027YCZZ	AF		B	Crystal (CSTCV18.43MXJ0H3-TC20(18.432MHz))	[X903]
28	RCRMC1028YCZZ	AE		B	Crystal (CSTCW (24.6MHz))	[X902]
29	RCRSC1016YCZZ	AG		B	Crystal (SM-26F(TypeB) 32.768KHz)	[X101]
30	RCRSC1023YCZZ	AK		B	Crystal (3.6864MHz(FCX-01L/REVER))	[X102]
31	RC-SZ0003YCZZ	AH		C	Capacitor (TEPSLC1A476M12R 47µ/10V(C))	[C822]
32	RC-SZ0004AWZZ	AC		C	Capacitor (10µ/10V(A) F931A106MAAASC)	[C614,C615,C632,C616,C633]
32	RC-SZ0004AWZZ	AC		C	Capacitor (10µ/10V(A) F931A106MAAASC)	[C503,C510,C511,C512,C657]
32	RC-SZ0004AWZZ	AC		C	Capacitor (10µ/10V(A) F931A106MAAASC)	[C330,C653]
33	RC-SZ0005YCZZ	AF		C	Capacitor (PSLA0G476M 47µ/4V(A))	[C104]
34	RC-SZ0006YCZZ	AK		C	Capacitor (TEPSLC0J107M12R 100U/6.3V(C))	[C401]
35	RFiLN1006YCZZ	AG		C	Noise filter (FS16TR)	[L606]
36	RH-iX2888AFZZ	AL		B	IC (IR3E3014)	[IC309]
37	RMPTR2101QCJJ	AB		B	Block resistir (100Ω×2(1005))	[BR601]
38	RMPTR2102QCJJ	AB		B	Block resistor (1KΩ×2)(1005)	[BR906]
39	RMPTR2103QCJJ	AB		B	Block resistor (10KΩ×2)	[BR503,BR604,BR306]
40	RMPTR2104QCJJ	AB		B	Block resistor (100KΩ×2)	[BR406,BR407]
41	RMPTR2220QCJJ	AC		B	Block resistor (22Ω×2)	[BR109,BR305]

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
42	RMPTR2223QCJJ	AB		B	Block resistor (22KΩ×2(1005))	[BR704]
43	RMPTR2473QCJJ	AC		B	Block resistor (47KΩ×2)	[BR806,BR402]
44	RMPTR2474QCJJ	AC		B	Block resistor (470KΩ×2)	[BR504,BR603,BR803,BR807,BR403]
	RMPTR2474QCJJ	AC		B	Block resistor (470KΩ×2)	[BR901,BR903,BR907]
45	RMPTR4102ACZZ	AB		B	Block resistor (4×1KΩ(1005))	[BR602,BR707,BR706,BR702]
46	RMPTR4104ACZZ	AB		B	Block resistor (100KΩ×4)(MNR04M0ABJ104)	[BR401]
47	RMPTR4105ACZZ	AB		B	Block resistor (1MΩ×4(1005))	[BR111,BR110,BR112,BR113,BR114]
48	RMPTR4220ACZZ	AB		B	Block resistor (22Ω×4)	[BR101,BR102,BR103,BR104,BR105]
	RMPTR4220ACZZ	AB		B	Block resistor (22Ω×4)	[BR106,BR107,BR108,BR301,BR302]
	RMPTR4220ACZZ	AB		B	Block resistor (22Ω×4)	[BR303,BR304]
49	RMPTR4223ACZZ	AB		B	Block resistor (22KΩ×4(1005))	[BR701,BR703,BR705]
50	RMPTR4474ACZZ	AB		B	Block resistor (470KΩ×4)	[BR408,BR501,BR902,BR905,BR904]
51	VCCCCY1HH101J	AA		C	Capacitor (50WV 100pF/1608Type/CH)	[C340]
52	VCCCCZ1HH101J	AA		C	Capacitor (50WV 100pF)	[C649]
53	VCCCCZ1HH300J	AA		C	Capacitor (50WV 30p(1005))	[C702]
54	VCCCCZ1HH470J	AA		C	Capacitor (50WV 47pF)	[C847]
55	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1.0μF)	[C351,C404,C409,C517,C648]
	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1.0μF)	[C651,C652,C660,C826,C830]
	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1.0μF)	[C836,C840,C846,C1011,C341]
	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1.0μF)	[C348,C349,C408,C622,C631]
	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1.0μF)	[C658,C819,C832,C901]
56	VCKYCY1AB224K	AC		C	Capacitor (10WV 0.22μF)	[C818]
57	VCKYCZ0JF105Z	AC		C	Capacitor (1μF/6.3V(1005))	[C101,C102,C103,C105,C106]
	VCKYCZ0JF105Z	AC		C	Capacitor (1μF/6.3V(1005))	[C107,C109,C110,C111,C112]
	VCKYCZ0JF105Z	AC		C	Capacitor (1μF/6.3V(1005))	[C202,C203,C209,C120,C121]
	VCKYCZ0JF105Z	AC		C	Capacitor (1μF/6.3V(1005))	[C663,C664,C844,C208,C849]
58	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C117,C118,C204@C122,C206,C210]
	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C301,C345,C119,C350,C352]
	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C353,C502,C509,C513,C518]
	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C609,C610,C611,C612,C650]
	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C637,C638,C641,C642,C643]
	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C701,C705,C708,C709,C828]
	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C829,C1012,C329,C334,C344]
	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C801,C803,C902,C903,C841,C904]
59	VCKYCZ1EB472K	AA		C	Capacitor (25WV 4700p(1005))	[C647]
60	VCKYCZ1EF223Z	AA		C	Capacitor (0.022μF/50V(1005))	[C505,C506,C507,C508]
61	VCKYCZ1HB102K	AA		C	Capacitor (50WV 1000pF)	[C661,C343]
62	VCKYTQ1AF106Z	AD		C	Capacitor (10μF/10V)(GRM42-6F106Z10PT)	[C810]
63	VCKYTQ1EB105K	AD		C	Capacitor (25WV 1.0μF)	[C354,C355,C356,C335,C336]
	VCKYTQ1EB105K	AD		C	Capacitor (25WV 1.0μF)	[C338,C339]
64	VCKYTV1AF475Z	AD		C	Capacitor (4.7μF/10V(2125)F)	[C608,C634,C635,C636]
65	VCSAFA1AJ106M	AD		C	Capacitor (10μF/10V(A))	[C108,C205,C207,C703,C331,C630]
66	VCSATA1DJ225M	AC		C	Capacitor (2.2μF/20V)	[C332]
67	VCSATE1AJ476M	AF		C	Capacitor (47μF/10V(B))	[C654,C655]
68	VHDDAN222//-1	AC		B	Diode (DAN222)	[D601,D801]
69	VHDFS1J3//-1	AD		B	Diode (FS1J3)	[D805]
70	VHDMA2ZD02/-1	AD		B	Diode (MA2ZD02)	[D1002]
71	VHDRB081L20-1	AG		B	Diode (RB081L20)	[D826]
72	VHDRB160M30-1	AD		B	Diode (RB160M-30TR)	[D829,D830,D831,D804,D827]
73	VHDRB471E//-1	AE		B	Diode (RB471E)	[D302,D303]
74	VHDRB520S30-1	AC		B	Diode (RB520S)	[D605,D832,D833]
75	VHDRB521S//-1	AD		B	Diode (RB521S-30)	[D1001]
76	VHDRB715F//-1	AF		B	Diode (RB715F)	[D603,D828]
77	VHERD3.6UH+-1	AD		B	Zener diode (RD3.6UH)	[D304]
78	VHi28F640FG-1	BH	N	B	64M FLASH ROM	[IC204]
79	VHi28F640FH-1	BH	N	B	64M FLASH ROM	[IC203]
80	VHi2F25J000-1	AV		B	LSI (SIL50752F25J000)(LOCOMO-QFP15-128PIN)	[IC901]
82	VHi752F26B0-1	AX		B	LSI (S1L50752F26B000)(SCOOP)	[IC401]
83	VHiLT1617-1-1	AQ		B	LSI (LT1617ES8-1#TR)(LT1617-1)	[IC305]
84	VHiLTC17314-1	AR		B	LSI (LTC1731EMS8-4.2-T2)	[IC801]
85	VHiLZ9GG314-1	AQ		B	LSI (LZ9GG314)	[IC306]
86	VHiM62332FP-1	AK		B	LSI (M62332FP)	[IC301]
87	VHiNJM2172+-1	AH		B	LSI (NJM2172)	[IC604]
88	VHiPCM1741+-1	AN		B	LSI (PCM1741)	[IC609]
89	VHiS80830LN-1	AD	N	B	IC (S80830ALNP)	[IC811]
90	VHiS80833LN-1	AD	N	B	IC (S80833ALNP)	[IC802]
91	VHiS80920ANMP	AF		B	IC (S80920ANMP)	[IC701]
92	VHiS80940AN-1	AD		B	IC (S80940ANMP)	[IC807]
94	VHiSP6650EU-1	AK	N	B	IC (SP6650)	[IC813,IC815]
95	VHiTC35143AF1	BA		B	IC (TC35143F-LQFP64-P-1010-0.50A)	[IC501]
96	VHiTC75S51U-1	AF		B	IC (TC75S51FU)	[IC611]
97	VHiTC7S02FU-1	AE		B	IC (TC7S02FU)	[IC613]
98	VHiTC7S14FU-1	AF		B	IC (TC7S14FU)	[IC814]
99	VHiTC7S66U/-1	AE		B	IC (TC7S66U)	[IC607,IC610]
100	VHiTC7SET08FU	AE		B	IC (TC7SET08FU)	[IC302]
101	VHiTC7SH08U-1	AE		B	IC (TC7SH08FU)	[IC703,IC310,IC205]
102	VHiTC7W00FK-1	AE		B	IC (TC7W00FK)	[IC102]
103	VHiTC7W66FK-1	AF		B	IC (TC7W66FK)	[IC606,IC608]
104	VHiTEA1206T-1	AQ	N	B	IC (TEA1206T)	[IC816]
105	VHiTK11131C-1	AE		B	IC (TK11131CS)	[IC1004,IC603]

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
106	VHiTK11133C-1	AE		B	IC (TK11133CS)	[IC502,IC308,IC605]
107	VHPGP2W0110-1	AN		B	IR unit (GP2W0110YP)	[IR701]
108	VHPLT1F67AF-1	AC		B	LED (LT1F67AF)	[LED901]
109	VHPLT1H67A+-1	AC		B	LED (LT1H67A (D))	[LED801]
110	VRN-CZ1JD472D	AA	N	C	RESITOR (4.7K(1005)D)	[R812,R813]
111	VRS-CY1JB240J	AA		C	Resistor (1/16W 24Ω ±5%(1608))	[R612,R613]
112	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)(Jumper/1608Type)	[R501,F701,F808,F810,R629]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)(Jumper/1608Type)	[R630,F807,F811,F812,F301]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)(Jumper/1608Type)	[RF302,F303,F601]
113	VRS-CY1JD100J	AA		C	Resistor (1/16W 10Ω ±5%)	[R713]
114	VRSCY1JD1962F	AA		C	Resister (1/16W 19.6kΩ ±1%((1608))	[R824]
115	VRSCY1JD2492F	AA		C	Resister (1/16W 24.9KΩ ±1%((1608))	[R308]
116	VRS-CY1JD471F	AB		C	Resister (1/16W 470Ω ±1%)	[R855]
117	VRS-CY1JR134D	AA		C	Resister (1/16W 130KΩ ±0.5%(1608))	[R852,R862]
118	VRS-CY1JR304D	AA		C	Resistor (1/16W 300kΩ ±0.5%)	[R851]
119	VRS-CY1JR433D	AA		C	Resistor (1/16W 43kΩ ±0.5%)	[R853]
120	VRS-CY1JR473D	AA		C	Resistor (1/16W 47KΩ ±0.5%)	[R861]
121	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R103,R104,R125,R126,R202]
	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R203,R205,R207,R213,R310]
	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R318,R325,R328,R403,R518]
	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R606,R635,R658,R709,R864]
	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R321,R401,R402,R514,R637]
	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R901,R903,R906,R909,R911]
	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R657,R659,R912,R516]
122	VRS-CZ1JB100J	AA		C	Resistor (1/16W 10Ω ±5%(1005))	[R504,R506,R507,R508,R856]
	VRS-CZ1JB100J	AA		C	Resistor (1/16W 10Ω ±5%(1005))	[R860,R312,R703]
123	VRS-CZ1JB101J	AA		C	Resistor (1/16W 100Ω ±5%(1005))	[R907,R307,R622,R623,R624,R625]
124	VRS-CZ1JB102J	AA		C	Resistor (1/16W 1KΩ ±5%(1005))	[R608,R706,R843,R832,R404]
	VRS-CZ1JB102J	AA		C	Resistor (1/16W 1KΩ ±5%(1005))	[R306,R311,R702,R809,R823,R803]
125	VRS-CZ1JB103J	AA		C	Resistor (1/16W 10KΩ ±5%(1005))	[R303,R632,R505,R868,R639]
	VRS-CZ1JB103J	AA		C	Resistor (1/16W 10KΩ ±5%(1005))	[R701,R808,R842,R908,R654]
	VRS-CZ1JB103J	AA		C	Resistor (1/16W 10KΩ ±5%(1005))	[R649,R655,R819,R829,R913]
126	VRS-CZ1JB104J	AA		C	Resistor (1/16W 100KΩ ±5%(1005))	[R105,R609,R665,R821,R841]
	VRS-CZ1JB104J	AA		C	Resistor (1/16W 100KΩ ±5%(1005))	[R707,R1007,R603,R301,R305,R1015]
127	VRS-CZ1JB105J	AD		C	Resistor (1/16W 1MΩ ±5%(1005))	[R611,R640,R610,R130,R133]
	VRS-CZ1JB105J	AD		C	Resistor (1/16W 1MΩ ±5%(1005))	[R135,R1016,R131,R132,R134]
	VRS-CZ1JB105J	AD		C	Resistor (1/16W 1MΩ ±5%(1005))	[R136,R302,R327,R902,R904,R905]
128	VRS-CZ1JB152J	AA		C	Resistor (1/16W 1.5KΩ ±5%(1005))	[R607]
129	VRS-CZ1JB153J	AD		C	Resistor (1/16W 15KΩ ±5%(1005))	[R317]
130	VRS-CZ1JB202J	AD		C	Resistor (1/16W 2KΩ ±5%(1005))	[R650,R645]
131	VRS-CZ1JB220J	AA		C	Resistor (1/16W 22Ω ±5%(1005))	[R511,R314,R315]
132	VRS-CZ1JB221J	AD		C	Resistor (1/16W 220Ω ±5%(1005))	[R651,R652]
133	VRS-CZ1JB273J	AD		C	Resistor (1/16W 27KΩ ±5%(1005))	[R517,R705]
134	VRS-CZ1JB274F	AB		C	Resistor (1/16W 270KΩ ±1%(1005))	[R309]
135	VRS-CZ1JB333J	AA		C	Resistor (1/16W 33kΩ ±5%(1005))	[R502,R503,R605,R616]
136	VRS-CZ1JB433J	AD		C	Resistor (1/16W 43KΩ ±5%(1005))	[R316]
137	VRS-CZ1JB472J	AA		C	Resistor (1/16W 4.7KΩ ±5%(1005))	[R1008,R601,R602,R664,R661,R662]
138	VRS-CZ1JB473J	AA		C	Resistor (1/16W 47KΩ ±5%(1005))	[R128,R633,R643,R1013,R801]
139	VRS-CZ1JB474J	AD		C	Resistor (1/16W 470KΩ ±5%(1005))	[R108,R109,R110,R111,R112]
	VRS-CZ1JB474J	AD		C	Resistor (1/16W 470KΩ ±5%(1005))	[R113,R114,R115,R127,R201]
	VRS-CZ1JB474J	AD		C	Resistor (1/16W 470KΩ ±5%(1005))	[R330,R405,R509,R838,R849]
	VRS-CZ1JB474J	AD		C	Resistor (1/16W 470KΩ ±5%(1005))	[R846,R837,R865,R304,R814]
	VRS-CZ1JB474J	AD		C	Resistor (1/16W 470KΩ ±5%(1005))	[R867,R866]
140	VRS-CZ1JB682J	AD		C	Resistor (1/16W 6.8KΩ ±5%(1005))	[R666]
141	VRS-CZ1JB822J	AD		C	Resistor (1/16W 8.2KΩ ±5%(1005))	[R667,R668]
142	VRS-CZ1JD104F	AA		C	Resistor (1/16W 100KΩ ±1%)	[R644,R646]
143	VRS-CZ1JD330J	AA		C	Resistor (1/16W 33Ω ±5%)	[R1009,R1010]
144	VRS-CZ1JD332J	AA		C	Resistor (1/16W 3.3KΩ ±5%)	[R1014]
145	VRS-CZ1JD362J	AA		C	Resistor (1/16W 3.6KΩ ±5%)	[R322]
146	VRS-CZ1JD623J	AA		C	Resistor (1/16W 62KΩ ±5%)	[R319]
147	VRS-TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%)	[R204]
148	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R804,R833]
149	VRS-TS2ELR15F	AC		C	Transistor (1/4W 0.15Ω ±1%(2125))	[R806]
150	VS2SJ243//-1	AD		B	Transistor (2SJ243)	[Q601,Q1005]
151	VS2SK3019++-1	AC		B	Transistor (2SK3019)	[Q501,Q902,Q828,Q302,Q807,Q901]
152	VS3LP01S+++-1	AC	N	B	Transistor (3LP01S)	[Q827,Q829]
153	VS3LP02M+++-1	AC		B	FET (3LP02M)	[Q608]
154	VSDTC144EU/-1	AB		B	Transistor (DTC144EU)	[Q602,Q815]
155	VSFDC6303N+-1	AF		B	FET (FDC6303N)	[Q605]
156	VSFDC634P//-1	AF		B	Transistor (FDC634P)	[Q801,Q825,Q830,Q303,Q805]
	VSFDC634P//-1	AF		B	Transistor (FDC634P)	[Q810,Q824]
157	VSUMF6N++++-1	AD		B	Transistor (UMF6N)	[Q609,Q804,Q1004]
158	VSUPA1850++-1	AG		B	FET (UPA1850(P-DUAL))	[Q802]
159	VSUPA572T//-1	AC		B	Transistor (UPA572T)	[Q1003,Q820,Q301]
160	VSXP135A114-1	AH		B	FET (XP135A1145SR)	[Q304]
200	KMEC-1013YCZZ	AN		D	CF connector frame	[CN401]
201	PTPEH1108YCZZ	AB		D	CF tape	
202	PZETL1074YCZZ	AD		C	PWB insulation tape	
203	PZETL1079YCZZ	AD		C	Battery section insulation sheet	
204	QCNCW1339AC0C	AG		C	AC adapter jack (3pin)(HEC3600-010010)	[CN802]

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
205	QJAKC1015YCZZ	AF		C	Stereo headphone jack	[CN603]
206	QTANB1051YCZZ	AR		C	Contact spring unit	[CN701,CN702]
207	VHDDSP10G++-1	AD	N	B	Diode	[D802,D824]
208	VRS-CZ1JB470J	AA		C	Resistor (1/16W 47Ω ±5%(1005))	[R313]
	(Unit)					
901	DUNTK2247YCZZ	CE	N	E	Main PWB unit	

4 Sub PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	QCNCM1111YC20	AH		C	Connector (2.020DP)	[CN1001]
2	QCNCW1108YC13	AP		C	Connector (SG1V013S1BE400)	[CN1002]
3	RALMB1003YCZZ	AM		B	Buzzer (EAF8RM11)	[SP]
4	RCiLZ1079YCZZ	AD		C	Coil (LQH3C470K34)	[L1001]
5	RC-KZ2241RC1A	AB		C	Capacitor (10WV 0.22μF)	[C1013]
6	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1.0μF)	[C1003]
7	VCKYCZ1CF104Z	AB		C	Capacitor (16WV 0.10μF)	[C1008,C1014,C1006]
8	VCSAFA1AJ106M	AD		C	Capacitor (10μF/10V(A))	[C1005,C1009,C1010]
9	VHDMA2ZD02/-1	AD		B	Diode (MA2ZD02)	[D1005,D1006,D1003]
10	VHDRB520S30-1	AC		B	Diode (RB520S)	[D1002]
11	VHiMM3005FN-1	AF		B	IC (MM3005FNRE)	[IC1003]
12	VHiS80920ANMP	AF		B	IC (S80920ANMP)	[IC1002]
13	VHiTK11133C-1	AE		B	IC (TK11133CS)	[IC1001]
14	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)(Jumper/1608Type)	[F1001,R1006]
15	VRS-CY1JD104J	AA		C	Resistor (1/16W 100KΩ ±5%)	[R1020]
16	VRS-CZ1JB000J	AA		C	Resistor (1/16W 0Ω ±5%(1005))	[R1015,R1016]
17	VRS-CZ1JB102J	AA		C	Resistor (1/16W 1KΩ ±5%(1005))	[R1011]
18	VRS-CZ1JB104J	AA		C	Resistor (1/16W 100KΩ ±5%(1005))	[R1017,R1018,R1019]
19	VRS-CZ1JB105J	AD		C	Resistor (1/16W 1MΩ ±5%(1005))	[R1002,R1003,R1004,R1005,R1012]
20	VS2SD2351W/-1	AC		B	Transistor (2SD2351)	[Q1004]
21	VS2SK3019++-1	AC		B	Transistor (2SK3019)	[Q1002]
	(Unit)					
901	DUNTK2249YCS1	BA	N	E	Sub PWB unit	

5 Key PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	QSW-K0237AFZZ	AC		B	Tact switch	[KS08,KS09,KS17,KS18,KS19]
2	QSW-K0237AFZZ	AC		B	Tact switch	[KS27,KS29,KS37,KS38,KS39]
3	QSW-K0237AFZZ	AC		B	Tact switch	[KS47,KS48]
	(Unit)					
901	DUNTK2249YCS2	AR	N	E	Key PWB unit	

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